FAST-40 NOISE MARGIN

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ASSUMPTIONS:

- Receiver sensitivity = +/- 30mv @ 40.0Mhz
  = +/- 20mv @ 0.1Mhz

- Terminator offset = 100 - 130mv favoring negation

- Terminator resistance = 100 - 115 ohms

- Line impedence = 85 (loaded)
  = 110 - 135 ohms (unloaded)

- Drive currents: Balanced is compared to unbalanced 2:1

- Incident wave voltages are calculated for attenuations of 0, -1, and -2 decibel.

TRANSITION CASES:

#	start state	end state	
1	active negation	passive bus	Bus release
2	assertion	passive bus	Wired Or release
3	active negation	assertion	high speed transition
4	assertion	active negation	high speed transition
5	passive bus	assertion	Wired Or (not shown)
6	passive bus	active negation	(not shown)

FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #1

DRIVEN NEGATION ---> HIGH IMPEDENCE NEGATION (Bus Release):

```
V1 = Quiescent Negated voltage--------------------
                                ^         ^
                                |         |  Vswing = Zline * Ineg/2
                                |         |
         driven voltage         |         |
         Vdrv = Ineg * Rterm/2  |       __v_______________
                                |         ^
        ----------------  100mv |         |  noise margin
                                |         V
                                |       ----------------------   Vdiff = 20mv
         terminator             |
          offset= 100-130mv     |       rvcr sensitivity = 20mv
                                v
Vdiff=0 ---------------------------------------------------------    Vdiff = 0
```

V1 = Vneg + Ineg * Rterm / 2
Vswing = Zline * Ineg / 2
V2 = V1 - Vswing

worst case:

Vterm	min	100 mv
Rterm	min	100 ohms
Zline	max	135 ohms
Ineg	max	-

Vterm	Rterm	Zline	Ineg	V0	Vsw1	V1	-1 db	-2 db	Vfinal
-100	100	135	3.75	-287	253	- 34	-62	-86	-100
-100	100	135	4.5	-325	303	- 22**	-55	-84	-100
-100	100	135	9	-550	607	+ 57**	-9**	-68	-100
-100	100	135	16	-900	1080	+180**	+62**	-44	-100

Conclusions:

1 There is no margin for ringing or crosstalk when active negation is turned off.
2 Protocol chip logic must tolerate bus release glitches lasting for a bus round trip time.
3 Problem is worst near the source, and gets better with attenuation.

FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #2

ASSERTED --> PASSIVE NEGATED (WIRED OR Release):

```
    Incident wave negated voltage ________________________________
                                        ^                        ^
                                        |       noise margin     |
                                        |                        v
                                        |       ------------------------- 75mv
                                        |       crosstalk allowance = 35mv
                                        |       ------------------------- 40mv
           -------------------------    |
          Terminator offset = 0    ^    |       Rcvr sensitivity = 40mv
 Vdiff = 0 _______________________|_____|____________________________ Vdiff =
0
                                   |     |
           Vdrv = Iasr * Rterm/2   |     | Vswing
                                   |     |
 Quiescent Asserted voltage ______v_____v
```

V1 = Vterm + Iasr * Rterm / 2
Vsw = Zline * (Iasr / 2)
V1 = V0 - Vswing

	Worst case		Best case	
Vterm	min	100 mv	max	130 mv
Rterm	max	115 ohms	min	100 ohms
Zline	min	85 ohms	max	135
Iassert	max	-	min	-

ASSERTION --> Passive NEGATION

Vterm	Rterm	Zline	Iassert	V0	Vsw	V1	-1 db	-2 db	Vfinal
Worst case:									
-100mv	115	85	7.5ma	331mv	-318mv	+ 13**	+ 48**	+ 78**	-100mv
-100	115	85	9.0	417	-382	+ 35**	+ 77**	+114**	-100
-100	115	85	16	820	-680	+140**	+216**	+280**	-100
Best case:									
-130	100	135	7.5	245	-506	-261	-206	-157	-100
-130	100	135	9.0	320	-607	-287	-221	-162	-100
-130	100	135	16	670	-1080	-410	-292	-188	-100

Conclusions:

1. Best case and worst case bracket the threshold, so typical cases are indeterminate.
2. Wired OR release transitions are NOT guaranteed to cleanly negate on the incident wave.
3. Protocol chips must tolerate “Wired Or” releases which flutter about threshold for a bus round trip time.
4. The lack of hysteresis on the LVD receivers may create new issues to be dealt with in the protocolchip logic.
5. Attenuation aggravates this problem.

FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #3

DRIVEN NEGATED --> ASSERTED:

```
        -------------------------- Quiescent Negated voltage = V1
         driven voltage          ^
         Vdrv = Ineg * Rterm/2   |
        ----------------  130mv  |
         terminator              |
          offset= 100-130mv      |
Vdiff=0 ------------------------|------------------------------   Vdiff = 0
                                |       rcvr sensitivity = 30mv
                          Vswing|       -------------------------     = -30mv
                                |         ^
                                |         | noise margin
        Incident asserted wave__v_________v_________________________ = V2
```

V0 = Vneg -Ineg * Rterm/2
Vswing = Zline * (Iasr/2 + Ineg/2)
Vfinal = (terminator offset) + Iasr * Rterm/2
Vincident_wave = V0 + Vswing

Worst case:		
Vterm	max	130mv
Rterm	max	115ohm
Zline	min	85ohm
Idrive	min	-

NEGATION --> ASSERTION

Vterm	Rterm	Zline	I+/-	V0	Vsw	Vinc	-1.0db	-2.0db	Vfinal
unbalanced:									
-130	115	85	6/3	-303mv	383mv	80mv	38mv	1**	215mv
-130m	115	85	7.5/3.75	-346	478	132	80	34	301
-130	115	85	8/4	-360	510	150	94	45	330
-130	115	85	9.4.5	-389	574	185	122	67	387
-130	115	85	10/5	-417	637	220	151	89	445
balanced:									
-130	115	85	9/9	-648	765	117	34	-40**	387
-130	115	85	10/10	-705	850	145	52	-30**	445
-130	115	85	12/12	-820	1020	200	89	-10**	560
-130	115	85	14/14	-935	1190	255	125	10**	675
-130	115	85	16/16	-1050	1360	310	162	30	790

Conclusion:

For a bus with 1 decibel of loss and/or crosstalk, a “balanced current driver” will require 2 times as much power as an “unbalanced current driver” with a ratio of 2:1 for Assertion : Negation currents.

For a bus with 2 decibels of loss and/or crosstalk, a “balanced current driver” will require 3 times as much power as an “unbalanced current driver” with a ratio of 2:1 for Assertion : Negation currents.

Loss	2:1 ratio	Balanced
1 db	6.0/3.0 - 7.5/3.75mA	9/9 - 11/11mA
2 db	7.5/3.75 - 9.0/4.5mA	16/16 - 19/19mA

FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #4

ASSERTED --> DRIVEN NEGATED:

```
    Incident wave negated voltage ________________________________
                                            ^                        ^
                                            |       noise margin     |
                                            |                        v
                                           |       ------------------------- 105mv
                                            |       crosstalk allowance = 35mv
                                            |       ------------------------- 70mv
           -------------------------        |
          Terminator offset = 0    ^        |       Rcvr sensitivity = 70mv
 Vdiff = 0 _______________________|______|____________________________ Vdiff =
0
                                   |      |
           Vdrv = I * Rterm/2      |      | Vswing
                                   |      |
 Quiescent Asserted voltage ______v_____v
```

V1 = Vterm + Iasr * Rterm/2
Vsw = Zline * (Iasr/2 + Ineg/2)
V1 = V0 - Vswing
Vincident_wave = V0 + Vswing

Worst case:			
	Vterm	min	100mv
	Rterm	max	115ohm
	Zline	min	85ohm
	Idrive	min	-

ASSERT --> NEGATE

Vterm	Rterm	Zline	I+/-	V0	Vsw	Vinc	-1.0db	-2.0db	Vfinal
unbalanced:									
-100m	115	85	6/3	275mv	-382mv	-107mv	- 65mv	- 28**	-272mv
-100m	115	85	7.5/3.75	331mv	-478mv	-147mv	- 95mv	- 49	-316
-100	115	85	8/4	360	-510	-150	- 94	- 45	-330
-100	115	85	9/4.5	418	-574	-156	- 93	- 38	-359
-100	115	85	10/5	475	-637	-162	- 92	- 31	-387
balanced:									
-100	115	85	10/10	475	-850	-375	-282	-200	-675
-100	115	85	16/16	820	-1360	-540	-392	-260	-1020

Conclusion:

No problems at the drive current targets determined by the Negation -> Assertion transition:

Loss	2:1 ratio	Balanced
1 db	6.0/3.0 - 7.5/3.75mA	9/9 - 11/11mA
2 db	7.5/3.75 - 9.0/4.5mA	16/16 - 20/20mA

Problem:
- Cable attenuation is only specified at 5Mhz, but the REQ/ACK pulses will run at 40Mhz.
- Available lossy transmission line models for Spice do not give credible results.

Worst case cable:
- 30 GA
- Single strand
- 110 ohms = minimum line impedence
- 12 meters long = 40 feet.

Analysis:
- Only simple skin effect considered
- Calculated frequency dependent resistances for relevant harmonics to 440Mhz.
- Used minimum unloaded cable impedence because loaded impedence of 85 ohms can only be achieved over a very short distance.
- Ignored stubs
- Assumed that terminators were far enough away to not be useful within the setup/hold window. (round trip time from either the driver or the receiver to a terminator is greater than 5ns)
- Total bus length ~ 13 meters.

Network:

```
115 ohm ----------+---------------------------------------+-------- 115 ohm
term.     110ohms | 110 ohm, 12 meter differential cable | 85 ohms  term.
          0.5m    |                                       | 0.5m
                  |                                       |
                driver                                 receiver
```

```
 Rskin(freq)
--\/\/\----+---------
           |
           /
Vin        \ 110    Vout
           / ohms
           \
           |
--\/\/\----+----------
 Rskin(freq)
```

The voltage ratio per unit length can be calculated as Vout/Vin.

The voltage ratio for the entire cable can be calculated as:

Ratio = (Vout/Vin)^n , where n= number of unit lengths

The unit of length can be made smaller (R goes down, n goes up) until the computed voltage ratio stops changing significantly.

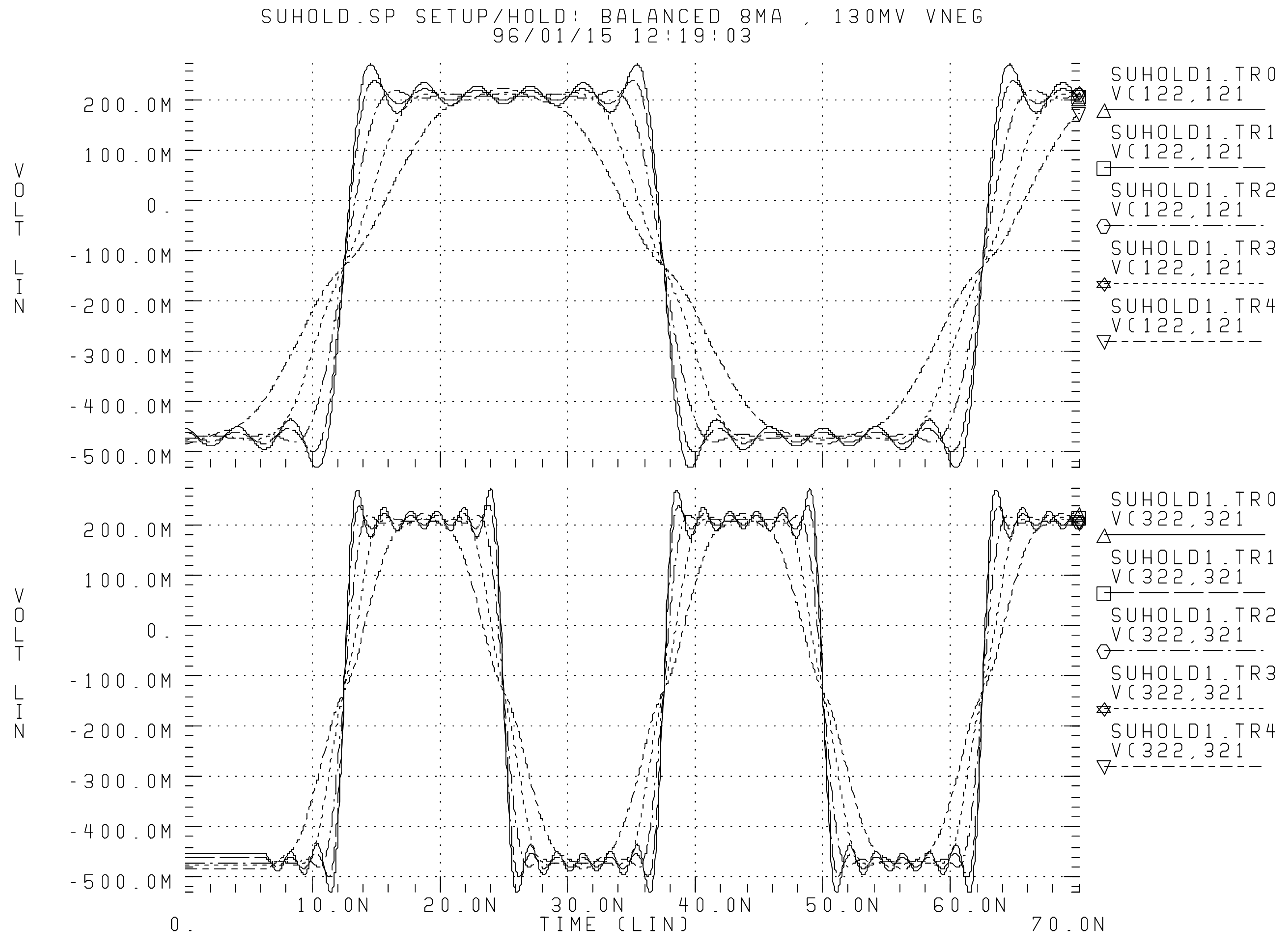
The result is a table of attenuation ratios versus frequency.

INPUT PULSE:
An idealized input waveform is transformed into a Fourier Series, resulting in a table of harmonic coefficients versus frequency.

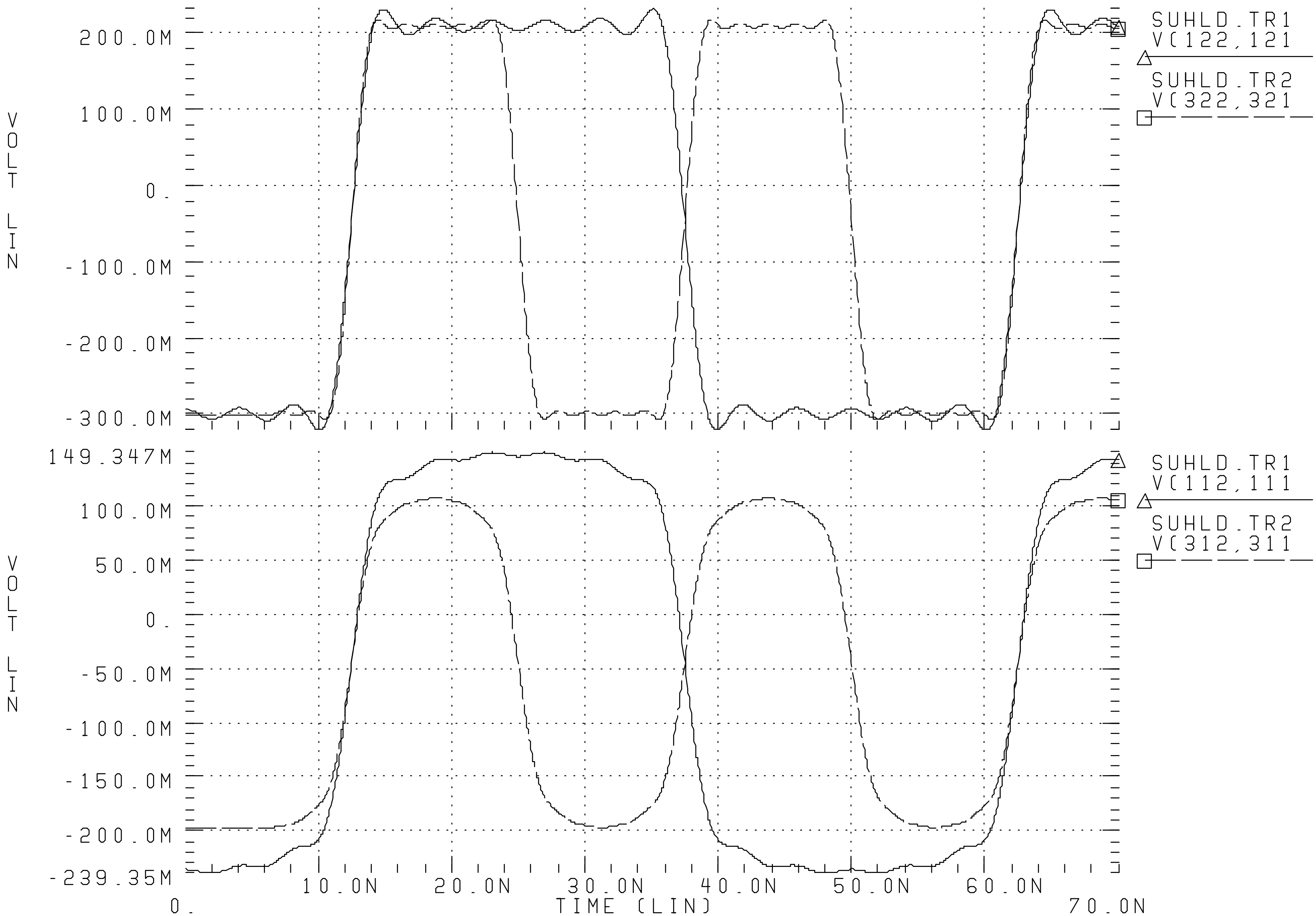
A sine wave generator is used for each harmonic with an amplitude equal to the product of the attenuation ratio and the harmonic coefficients. All sine wave generators are summed into a single node and then applied to the 85 ohm loaded line.

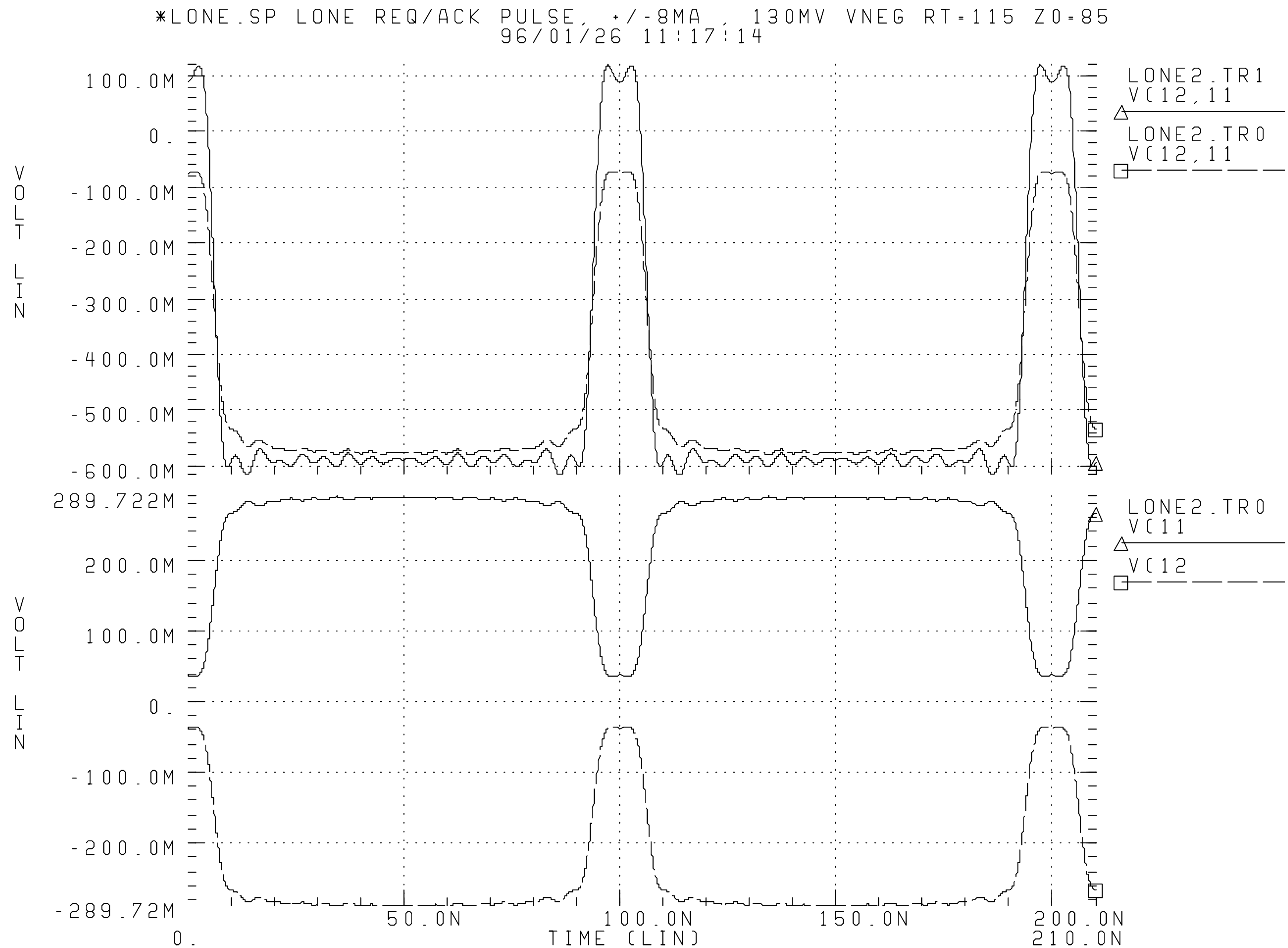
Three waveforms were studied:

- 40Mhz REQ/ACK square wave
- 20Mhz max data toggle rate
- 12.5ns REQ/ACK pulse at 10Mhz, to look at an isolated minimum width pulse

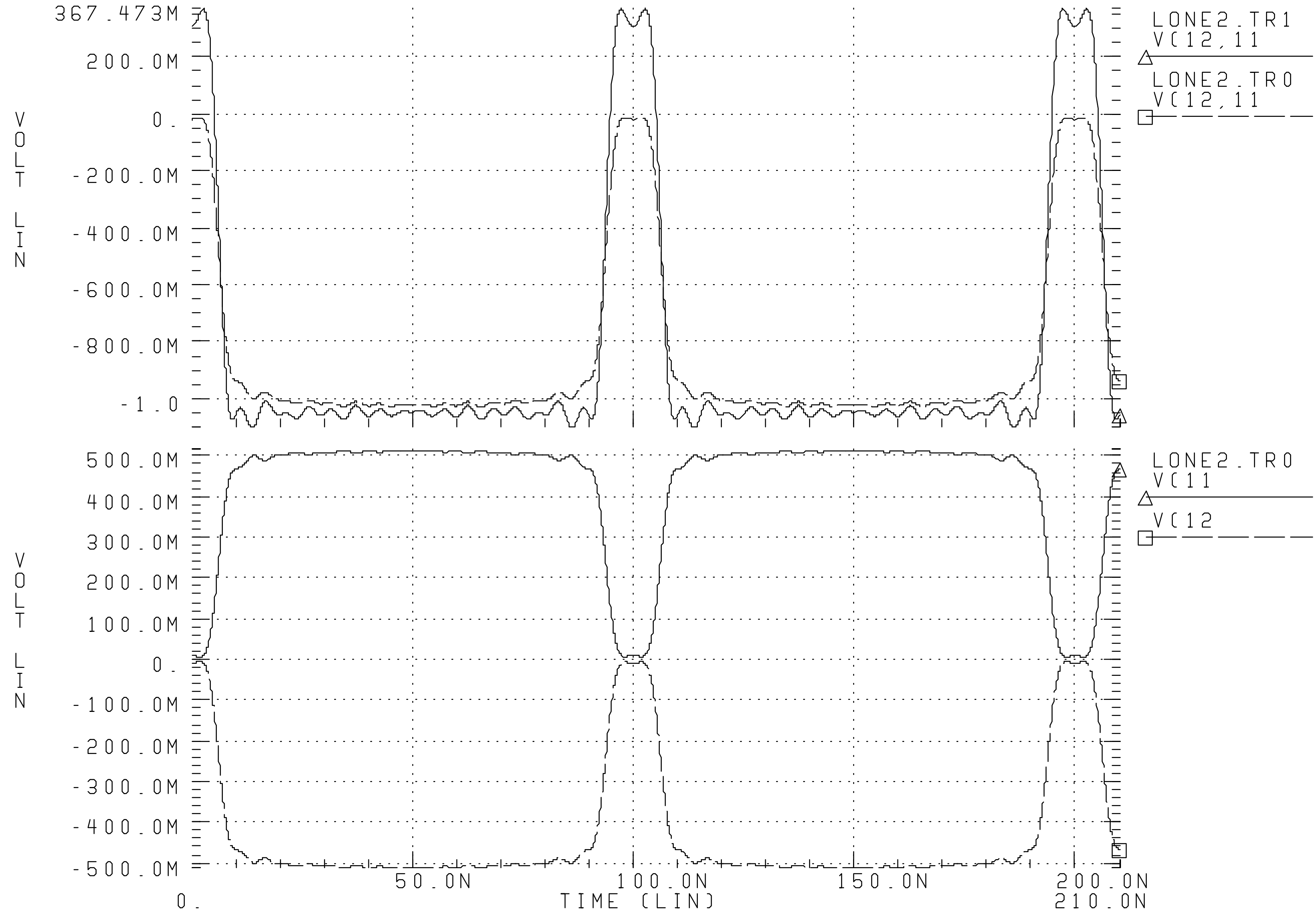

SUHOLD.SP SETUP/HOLD: BALANCED 8MA , 130MV VNEG
96/01/15 12:19:03
VOLT LIN
200.0M
100.0M
0.
-100.0M
-200.0M
-300.0M
-400.0M
-500.0M
SUHOLD1.TR0 V(122,121
SUHOLD1.TR1 V(122,121
SUHOLD1.TR2 V(122,121
SUHOLD1.TR3 V(122,121
SUHOLD1.TR4 V(122,121
SUHOLD1.TR0 V(322,321
SUHOLD1.TR1 V(322,321
SUHOLD1.TR2 V(322,321
SUHOLD1.TR3 V(322,321
SUHOLD1.TR4 V(322,321
0.
10.0N
20.0N
30.0N
40.0N
50.0N
60.0N
70.0N
TIME (LIN)

SUHOLD2.SP SETUP/HOLD: UNBALANCED 8MA/-4MA , 130MV VNEG
96/01/26 14:55:31

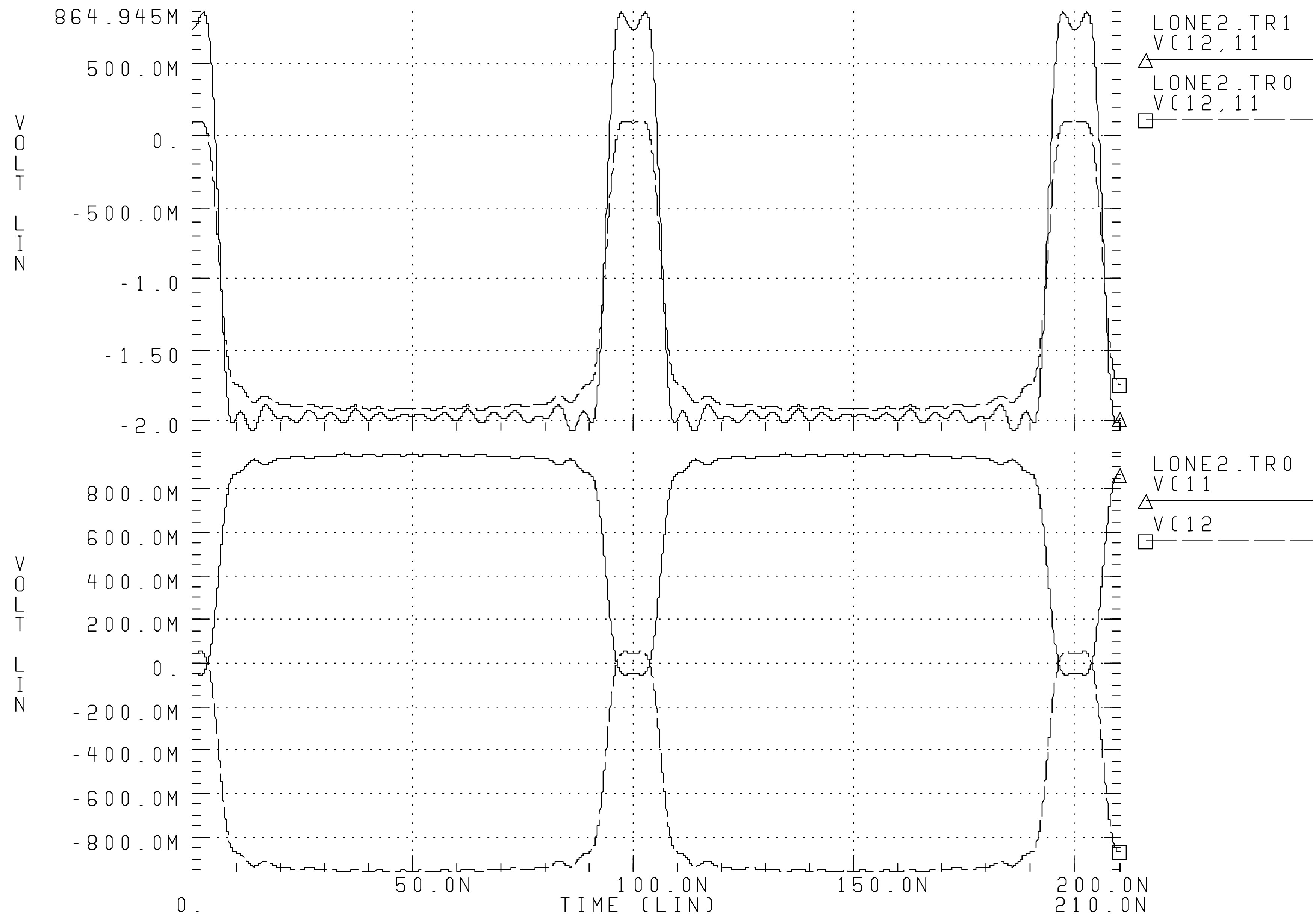


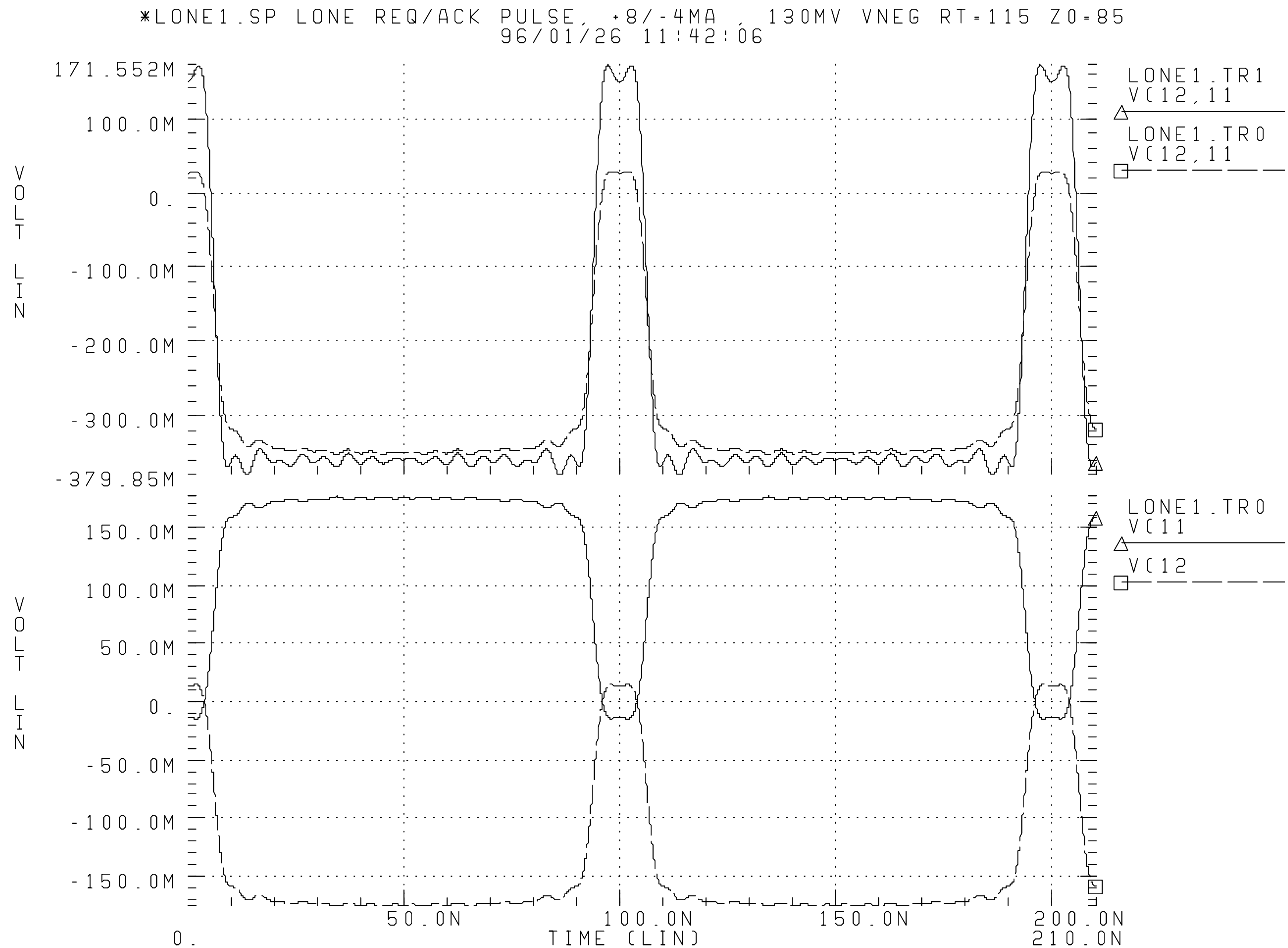

*LONE.SP LONE REQ/ACK PULSE, +/-8MA , 130MV VNEG RT=115 Z0=85
96/01/26 11:17:14
VOLT LIN
100.0M
0.
-100.0M
-200.0M
-300.0M
-400.0M
-500.0M
-600.0M
LONE2.TR1 V(12,11
LONE2.TR0 V(12,11
289.722M
200.0M
100.0M
0.
-100.0M
-200.0M
-289.72M
LONE2.TR0 V(11
V(12
0.
50.0N
100.0N
150.0N
200.0N
210.0N
TIME (LIN)

*LONE.SP LONE REQ/ACK PULSE, +/-16MA , 130MV VNEG RT=115 Z0=85
96/01/26 11:23:12



*LONE.SP LONE REQ/ACK PULSE, +/-32MA , 130MV VNEG RT=115 Z0=85
96/01/26 11:20:22




*LONE1.SP LONE REQ/ACK PULSE, +8/-4MA , 130MV VNEG RT=115 Z0=85
96/01/26 11:42:06
171.552M
100.0M
0.
-100.0M
-200.0M
-300.0M
-379.85M
VOLT LIN
150.0M
100.0M
50.0M
0.
-50.0M
-100.0M
-150.0M
VOLT LIN
0.
50.0N
100.0N
150.0N
200.0N
210.0N
TIME (LIN)
LONE1.TR1
V(12,11
LONE1.TR0
V(12,11
LONE1.TR0
V(11
V(12