ASSUMPTIONS:

- Receiver sensitivity = +/- 30mv @ 40.0Mhz
  = +/- 20mv @ 0.1Mhz
- Terminator offset = 100 - 130mv favoring negation
- Terminator resistance = 100 - 115 ohms
- Line impedance = 85 (loaded)
  = 110 - 135 ohms (unloaded)
- Drive currents: Balanced is compared to unbalanced 2:1
- Incident wave voltages are calculated for attenuations of 0, -1, and -2 decibel.

TRANSITION CASES:

<table>
<thead>
<tr>
<th>#</th>
<th>start state</th>
<th>end state</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>active negation</td>
<td>passive bus</td>
</tr>
<tr>
<td>2</td>
<td>assertion</td>
<td>passive bus</td>
</tr>
<tr>
<td>3</td>
<td>active negation</td>
<td>assertion</td>
</tr>
<tr>
<td>4</td>
<td>assertion</td>
<td>active negation</td>
</tr>
<tr>
<td>5</td>
<td>passive bus</td>
<td>assertion</td>
</tr>
<tr>
<td>6</td>
<td>passive bus</td>
<td>active negation</td>
</tr>
</tbody>
</table>
FAST-40 NOISE MARGIN CASES
 Incident wave transitions, case #1

DRIVEN NEGATION ---> HIGH IMPEDENCE NEGATION (Bus Release):

\[ V_1 = \text{Quiescent Negated voltage} \]
\[ V_{\text{swing}} = Z_{\text{line}} \times \frac{I_{\text{neg}}}{2} \]
\[ V_{\text{drv}} = \frac{I_{\text{neg}} \times R_{\text{term}}}{2} \]
\[ V_{\text{term}} = 100\text{mv} \]
\[ \text{rvcr sensitivity} = 20\text{mv} \]
\[ V_{\text{diff}} = 20\text{mv} \]

\[ V_{\text{diff}} = 0 \]

\[ V_1 = V_{\text{neg}} + \frac{I_{\text{neg}} \times R_{\text{term}}}{2} \]
\[ V_{\text{swing}} = Z_{\text{line}} \times \frac{I_{\text{neg}}}{2} \]
\[ V_2 = V_1 - V_{\text{swing}} \]

\begin{tabular}{cccccccccc}
Vterm & Rterm & Zline & Ineg & V0 & Vsw1 & V1 & -1 db & -2 db & Vfinal \\
-100 & 100 & 135 & 3.75 & -287 & 253 & -34 & -62 & -86 & -100 \\
-100 & 100 & 135 & 4.5 & -325 & 303 & -22** & -55 & -84 & -100 \\
-100 & 100 & 135 & 9 & -550 & 607 & +57** & -9** & -68 & -100 \\
-100 & 100 & 135 & 16 & -900 & 1080 & +180** & +62** & -44 & -100 \\
\end{tabular}

Conclusions:
1. There is no margin for ringing or crosstalk when active negation is turned off.
2. Protocol chip logic must tolerate bus release glitches lasting for a bus round trip time.
3. Problem is worst near the source, and gets better with attenuation.
FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #2

ASSERTED --> PASSIVE NEGATED (WIRED OR Release):

Incident wave negated voltage

\[ V_{diff} = 0 \]

\[ V_{drv} = I_{asr} \times R_{term}/2 \]

Quiescent Asserted voltage

\[ V_{1} = V_{term} + I_{asr} \times R_{term}/2 \]

\[ V_{sw} = Z_{line} \times (I_{asr} / 2) \]

\[ V_{sw} = V_{0} - V_{swing} \]

Worst case

<table>
<thead>
<tr>
<th>V_{term}</th>
<th>R_{term}</th>
<th>Z_{line}</th>
<th>I_{assert}</th>
<th>V_{0}</th>
<th>V_{sw}</th>
<th>V_{1}</th>
<th>-1 db</th>
<th>-2 db</th>
<th>V_{final}</th>
</tr>
</thead>
<tbody>
<tr>
<td>-100 mv</td>
<td>115</td>
<td>85</td>
<td>7.5 ma</td>
<td>331 mv</td>
<td>-318 mv</td>
<td>+13** +48** +78** -100 mv</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>9.0</td>
<td>417</td>
<td>-382</td>
<td>+35** +77** +114** -100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>16</td>
<td>820</td>
<td>-680</td>
<td>+140** +216** +280** -100</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Best case:

<table>
<thead>
<tr>
<th>V_{term}</th>
<th>R_{term}</th>
<th>Z_{line}</th>
<th>I_{assert}</th>
<th>V_{0}</th>
<th>V_{sw}</th>
<th>V_{1}</th>
<th>-1 db</th>
<th>-2 db</th>
<th>V_{final}</th>
</tr>
</thead>
<tbody>
<tr>
<td>-130</td>
<td>100</td>
<td>135</td>
<td>7.5</td>
<td>245</td>
<td>-506</td>
<td>-261</td>
<td>-206</td>
<td>-157</td>
<td>-100</td>
</tr>
<tr>
<td>-130</td>
<td>100</td>
<td>135</td>
<td>9.0</td>
<td>320</td>
<td>-607</td>
<td>-287</td>
<td>-221</td>
<td>-162</td>
<td>-100</td>
</tr>
<tr>
<td>-130</td>
<td>100</td>
<td>135</td>
<td>16</td>
<td>670</td>
<td>-1080</td>
<td>-410</td>
<td>-292</td>
<td>-188</td>
<td>-100</td>
</tr>
</tbody>
</table>

Conclusions:

1 Best case and worst case bracket the threshold, so typical cases are indeterminate.
2 Wired OR release transitions are NOT guaranteed to cleanly negate on the incident wave.
3 Protocol chips must tolerate “Wired Or” releases which flutter about threshold for a bus round trip time.
4 The lack of hysteresis on the LVD receivers may create new issues to be dealt with in the protocol chip logic.
5 Attenuation aggravates this problem.
FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #3

DRIVEN NEGATED --> ASSERTED:

\[ V_{diff} = 0 \]
\[ V_{swing} = V_{term} \]
\[ V_{final} = (\text{terminator offset}) + I_{asr} \times \frac{R_{term}}{2} \]

Worst case: $V_{term}$ max 130mv
$R_{term}$ max 115ohm
$Z_{line}$ min 85ohm
$I_{drive}$ min -

Conclusion:
For a bus with 1 decibel of loss and/or crosstalk, a “balanced current driver” will require 2 times as much power as an “unbalanced current driver” with a ratio of 2:1 for Assertion : Negation currents.

For a bus with 2 decibels of loss and/or crosstalk, a “balanced current driver” will require 3 times as much power as an “unbalanced current driver” with a ratio of 2:1 for Assertion : Negation currents.

<table>
<thead>
<tr>
<th>Loss</th>
<th>2:1 ratio</th>
<th>Balanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 db</td>
<td>6.0/3.0</td>
<td>7.5/3.75mA 9/9 - 11/11mA</td>
</tr>
<tr>
<td>2 db</td>
<td>7.5/3.75</td>
<td>9.0/4.5mA  16/16 - 19/19mA</td>
</tr>
</tbody>
</table>
FAST-40 NOISE MARGIN CASES
Incident wave transitions, case #4

ASSERTED --> DRIVEN NEGATED:

Incident wave negated voltage

\[ V_{diff} = 0 \]

\[ V_{drv} = I \cdot \frac{R_{term}}{2} \]

\[ V_{quiescent \, asserted} \]

\[ V_1 = V_{term} + I_{asr} \cdot \frac{R_{term}}{2} \]

\[ V_{sw} = Z_{line} \cdot \left( \frac{I_{asr}}{2} + \frac{I_{neg}}{2} \right) \]

\[ V_{1} = V_{0} - V_{swing} \]

\[ V_{incident \, wave} = V_{0} + V_{swing} \]

Worst case:

<table>
<thead>
<tr>
<th>Vterm</th>
<th>Rterm</th>
<th>Zline</th>
<th>I+/–</th>
<th>V0</th>
<th>Vsw</th>
<th>Vinc</th>
<th>-1.0db</th>
<th>-2.0db</th>
<th>Vfinal</th>
</tr>
</thead>
<tbody>
<tr>
<td>-100m</td>
<td>115</td>
<td>85</td>
<td>6/3</td>
<td>275mv</td>
<td>-382mv</td>
<td>-107mv</td>
<td>65mv</td>
<td>28**</td>
<td>-272mv</td>
</tr>
<tr>
<td>-100m</td>
<td>115</td>
<td>85</td>
<td>7.5/3.75</td>
<td>331mv</td>
<td>-478mv</td>
<td>-147mv</td>
<td>95mv</td>
<td>49</td>
<td>-316</td>
</tr>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>8/4</td>
<td>360</td>
<td>-510</td>
<td>-150</td>
<td>94</td>
<td>45</td>
<td>-330</td>
</tr>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>9/4.5</td>
<td>418</td>
<td>-574</td>
<td>-156</td>
<td>93</td>
<td>38</td>
<td>-359</td>
</tr>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>10/5</td>
<td>475</td>
<td>-637</td>
<td>-162</td>
<td>92</td>
<td>31</td>
<td>-387</td>
</tr>
</tbody>
</table>

Balanced:

<table>
<thead>
<tr>
<th>Vterm</th>
<th>Rterm</th>
<th>Zline</th>
<th>I+/–</th>
<th>V0</th>
<th>Vsw</th>
<th>Vinc</th>
<th>-1.0db</th>
<th>-2.0db</th>
<th>Vfinal</th>
</tr>
</thead>
<tbody>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>10/10</td>
<td>475</td>
<td>-850</td>
<td>-375</td>
<td>-282</td>
<td>-200</td>
<td>-675</td>
</tr>
<tr>
<td>-100</td>
<td>115</td>
<td>85</td>
<td>16/16</td>
<td>820</td>
<td>-1360</td>
<td>-540</td>
<td>-392</td>
<td>-260</td>
<td>-1020</td>
</tr>
</tbody>
</table>

Conclusion:
No problems at the drive current targets determined by the Negation --> Assertion transition:

Loss 2:1 ratio Balanced
1 db 6.0/3.0 - 7.5/3.75mA 9/9 - 11/11mA
2 db 7.5/3.75 - 9.0/4.5mA 16/16 - 20/20mA
Problem:
- Cable attenuation is only specified at 5Mhz, but the REQ/ACK pulses will run at 40Mhz.
- Available lossy transmission line models for Spice do not give credible results.

Worst case cable:
- 30 GA
- Single strand
- 110 ohms = minimum line impedance
- 12 meters long = 40 feet.

Analysis:
- Only simple skin effect considered
- Calculated frequency dependent resistances for relevant harmonics to 440Mhz.
- Used minimum unloaded cable impedance because loaded impedance of 85 ohms can only be achieved over a very short distance.
- Ignored stubs
- Assumed that terminators were far enough away to not be useful within the setup/hold window. (round trip time from either the driver or the receiver to a terminator is greater than 5ns)
- Total bus length ~ 13 meters.

Network:

```
115 ohm --------------------------------------------- 115 ohm
term. 110ohms | 110 ohm, 12 meter differential cable | 85 ohms term.
0.5m | 0.5m
driver receiver
```
The voltage ratio per unit length can be calculated as $\frac{V_{out}}{V_{in}}$.

The voltage ratio for the entire cable can be calculated as:

$$\text{Ratio} = \left(\frac{V_{out}}{V_{in}}\right)^n,$$

where $n$ = number of unit lengths.

The unit of length can be made smaller ($R$ goes down, $n$ goes up) until the computed voltage ratio stops changing significantly.

The result is a table of attenuation ratios versus frequency.

**INPUT PULSE:**

An idealized input waveform is transformed into a Fourier Series, resulting in a table of harmonic coefficients versus frequency.

A sine wave generator is used for each harmonic with an amplitude equal to the product of the attenuation ratio and the harmonic coefficients. All sine wave generators are summed into a single node and then applied to the 85 ohm loaded line.

Three waveforms were studied:
- 40Mhz REQ/ACK square wave
- 20Mhz max data toggle rate
- 12.5ns REQ/ACK pulse at 10Mhz, to look at an isolated minimum width pulse