

1. ELECTRICAL CHARACTERISTICS

1.1 Generator characteristics

The fundamental characteristic of a LVD-SCSI generator is the generation of a first-step differential output voltage magnitude at the A and B interchange connections to the balanced media to achieve a minimum of ± 30 mV of differential input at any other bus interchange. The minimum assertion voltage required to do this is 285 mV while the minimum negation voltage is 250 mV. Other characteristics that affect system performance are the common-mode output voltage, the maximum differential output voltage, the output impedance, and the output signal wave shape.

The requirements that follow, define these characteristics in terms of the voltages and currents defined in figure 1.

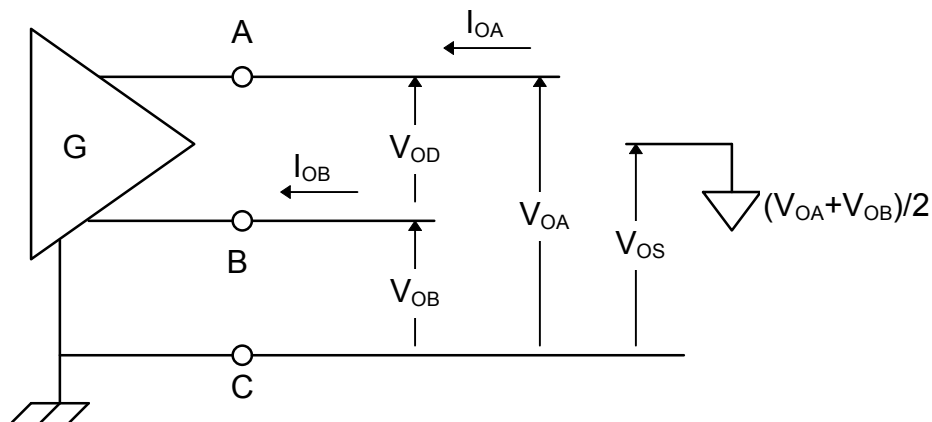


Figure 1 - Generator voltage and current definitions.

These requirements are for a generator only. See 5.3 for the characteristics of a combination Generator/Receiver (transceiver). The signaling sense of the voltages appearing across the is defined in figure 3 as follows:

- a. The A terminal of the generator shall be negative with respect to the B terminal for an Asserted state.
- b. The A terminal of the generator shall be positive with respect to the B terminal for a Negated state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

1.1.1 Differential output voltage, V_{OD}

To assure sufficient voltage to define a valid logic state at any interchange on a fully loaded LVD-SCSI bus a minimum differential output voltage must be generated. This value must be large enough that, after allowance for attenuation, reflections, and differential noise coupling, there is at least ± 30 mV across the interchange points connected to the LVD-SCSI bus. A minimum assertion level of ± 285 mV and a maximum negation level of 617 mV at the generator interchange allows for a loss of 70 mV of signal amplitude or 3 dB of attenuation, 55 mV of differential noise coupling, and 130 mV for bus reflections.

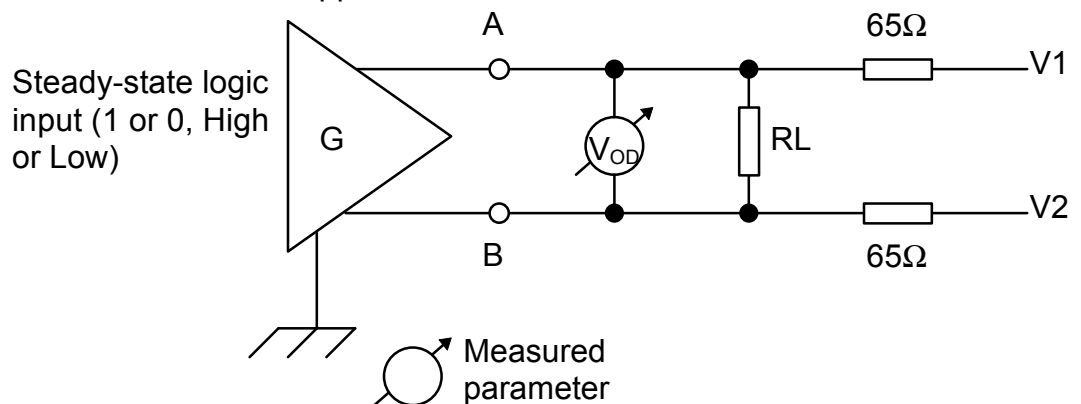
There must also be an upper limit to the differential output voltages to define the maximum voltage that can be attained at an interchange and assure a minimum negation level from assertion. A maximum negation level of 921 mV keeps the maximum differential voltage below 1050 mV after bus reflections. This maximum output, in conjunction with the generator/terminator common-mode outputs and allowable ground potential difference, shall maintain a voltage between 0 V and 2.5 V between any interchange point and its common. The maximum assertion level of 875 mV assures a the minumum negation level with a non-symmetrical driver.

The steady-state magnitude of the differential output voltage (V_{OD}), shall be comply with the limits and test conditions in table 1. For the opposite binary state, the polarity of V_{OD} shall be reversed (V_{OD}^*).

Table 1. Generator steady-state test limits and circuit parameters.

Test Parameter	Test Circuit (see figure 5)				Units	Tolerance
	1	2	3	4		
RL	95	95	140	140	Ohms	1%
V1	0.7	2.2	0.7	2.2	Volts	± 5 mV
V2	0.35	1.8	0.35	1.8	Volts	± 5 mV
V_{OD} maximum	NA	NA	875	875	mV	
V_{OD} minimum	285	285	NA	NA	mV	
V_{OD}^* maximum	617	617	921	921	mV	
V_{OD}^* minimum	250	250	NA	NA	mV	

Note: Table 2 represents the allowed ranges of common-mode voltage and differential load impedance on a LVD-SCSI bus. NA = not applicable.



Note: Resistors are $\pm 1\%$

Figure 2 - Differential steady-state output voltage test circuit.
1.1.2 Offset (common-mode output) voltage, V_{OS}

The steady-state magnitude of the generator offset voltage (V_{OS}), measured with the test load of figure 3 shall be greater than or equal to 0.525 V and less than or equal to 2 V for either binary state. The steady-state magnitude of the difference of V_{OS} for one binary state and V_{OS}^* , for the opposite binary state, shall be 16 mV or less.

$$0.529 \text{ V} \leq V_{OS} \leq 2 \text{ V}$$

$$0.529 \text{ V} \leq V_{OS}^* \leq 2 \text{ V}$$

$$|V_{OS} - V_{OS}^*| \leq 16 \text{ mV}$$

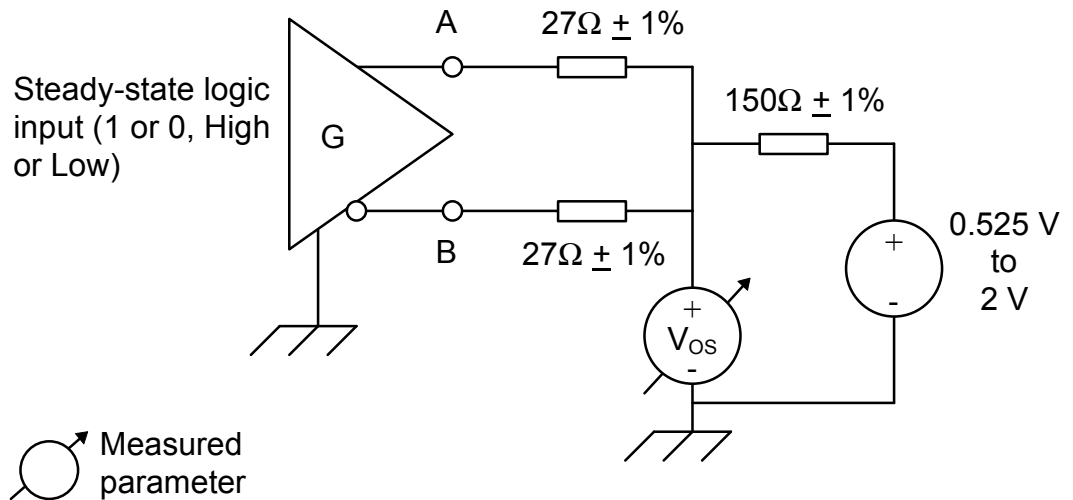


Figure 3 - Generator offset steady-state voltage test circuit.

1.1.3 Short-circuit currents, I_{OAS} and I_{OBS}

Since a LVD-SCSI bus allows multiple generators, the possibility of contention requires a restriction on the power that may be sourced to the interchange. This is accomplished with a maximum allowable current from the generator.

With the generator output terminals short-circuited to a variable voltage source, the magnitudes of the currents (I_{OAS} and I_{OBS}) shall not exceed 24 mA for either binary state (see figure 4) over a test voltage range of 0 V to 2.5 V.

$$|I_{OAS}| \leq 24.0 \text{ mA}$$

$$|I_{OBS}| \leq 24.0 \text{ mA}$$

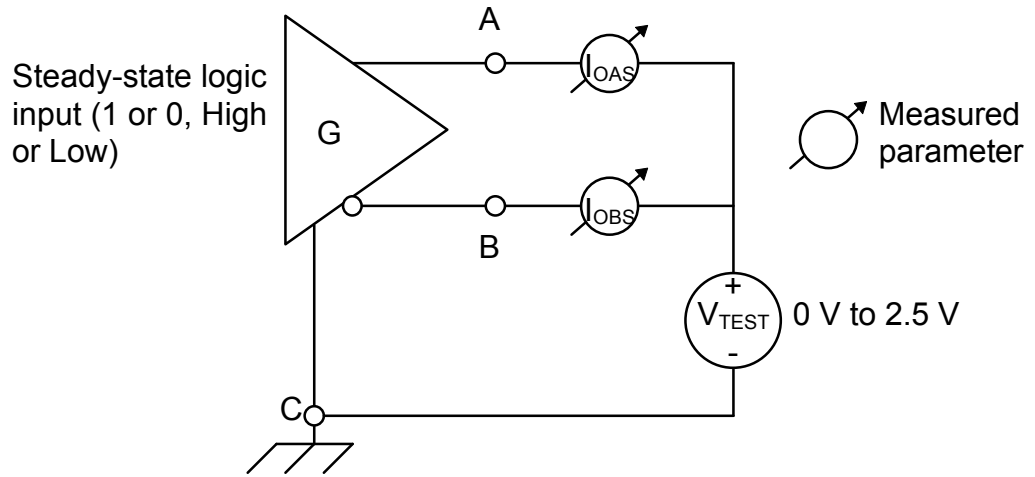


Figure 4 - Generator short-circuit test circuit.

1.1.4 Open-circuit output voltages, $V_{OA(OC)}$ and $V_{OB(OC)}$

To limit the maximum steady-state voltages at any interchange on the LVD-SCSI bus, the generator output voltage must be restricted. The highest output voltage occurs with no output current.

The voltage between each output terminal of the generator circuit and its common shall be between 0 V and 2.5 V when measured in accordance with figure 5. This requirement shall be met in all binary or Off states.

$$0\text{ V} \leq V_{OA(OC)} \leq 2.5\text{ V} \text{ and } 0\text{ V} \leq V_{OB(OC)} \leq 2.5\text{ V}$$

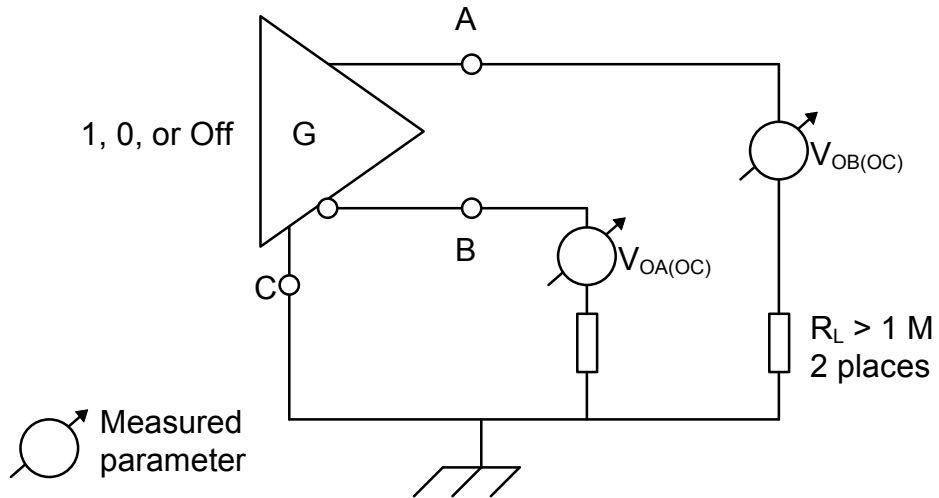


Figure 5 - Open-circuit output voltage test circuit.

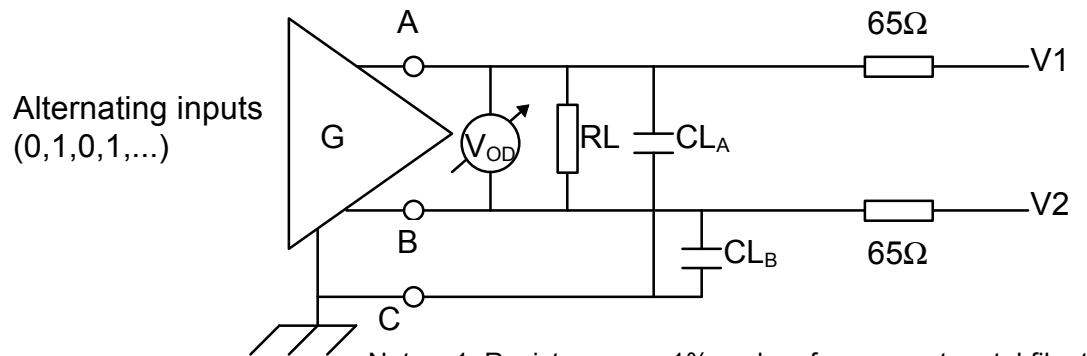
1.1.5 Output signal waveform

The differential output switching or transition time of a generator influences the maximum data rate and maximum stub lengths of a LVD-SCSI interface. Excessive over and under shoot of the output signal can cause electromagnetic emissions or false logic state changes on the media.

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured with the test circuit of figure 6 and table 2, shall be such that the voltage monotonically changes between 0.2 and 0.8 of the steady-state output, V_{SS} . V_{SS} is defined as the voltage difference between the two steady-state values of the generator output ($V_{SS} = |V_{OD}| + |V_{OD}^*|$).

The output signal rise or fall times between 0.2 and 0.8 of V_{SS} shall be between 0.26 ns and 3.75 ns.

The signal voltage shall not vary more than $\pm 20\%$ of the steady-state value until the next binary transition occurs. Measurement equipment used for compliance testing shall provide a bandwidth of 1 GHz minimum.



- Notes:
1. Resistors are $\pm 1\%$ and surface-mount metal film type.
 2. CL_A and CL_B are no more than 5 pF, include the instrumentation capacitance, and are equal within 0.5 pF.
 3. The longest physical dimension between the interchange points and any test circuit component shall be no greater than 0.1 m.
 4. V1 and V2 shall have a source impedance of less than 50 Ω from 0 Hz to 120 MHz.


 Measured parameter

Figure 6 - Differential output switching voltage test circuit.

Table 2. Generator switching test circuit parameters.

Test Parameter	Test Circuit				Units	Tolerance
	1	2	3	4		
RL	95	95	140	140	Ohms	1%
V1	1.2	1.6	1.2	1.6	Volts	± 5 mV
V2	0.85	1.3	.85	1.3	Volts	± 5 mV

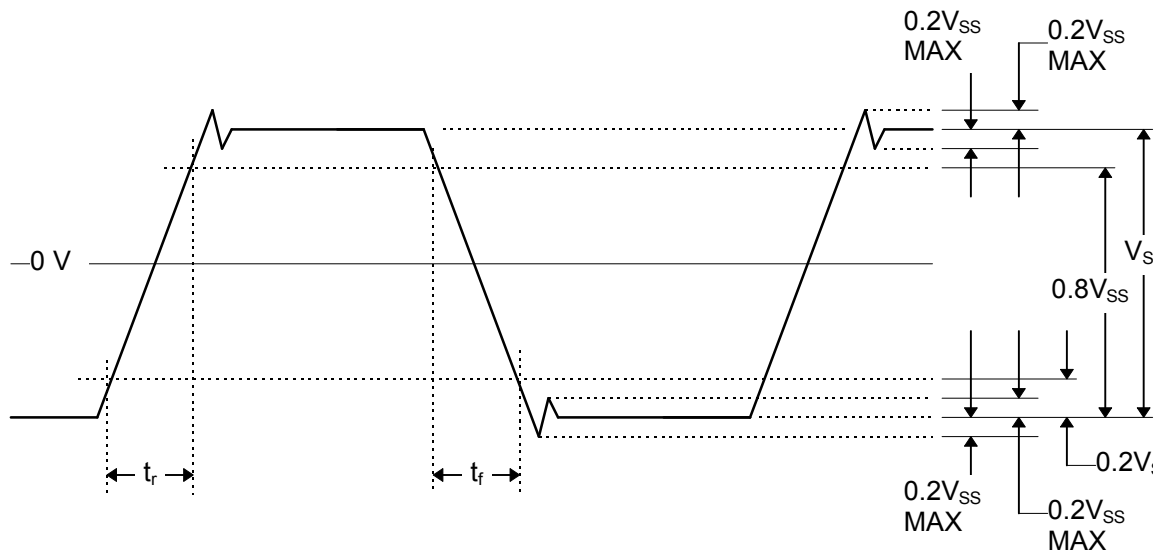


Figure 7. Generator output signal waveform.

1.1.6 Dynamic output signal balance, $V_{OS(PP)}$

A mismatch in the magnitude of rate at which the voltage changes at the A and B interchange points, results in a common-mode ac signal. This may cause electromagnetic emissions from the media, excursions outside the receivers' common-mode input voltage range, and/or differential noise. During transitions of the generator output between any state transition of high-to-low, low-to-high, high-to-off, off-to-high, low-to-off, or off-to-low, the resulting offset voltage (V_{OS}) measured with the test circuit shown in figure 7, shall not vary more than 50 mVpp (peak-to-peak). Measurement equipment used for compliance testing shall provide a bandwidth of 300 MHz minimum.

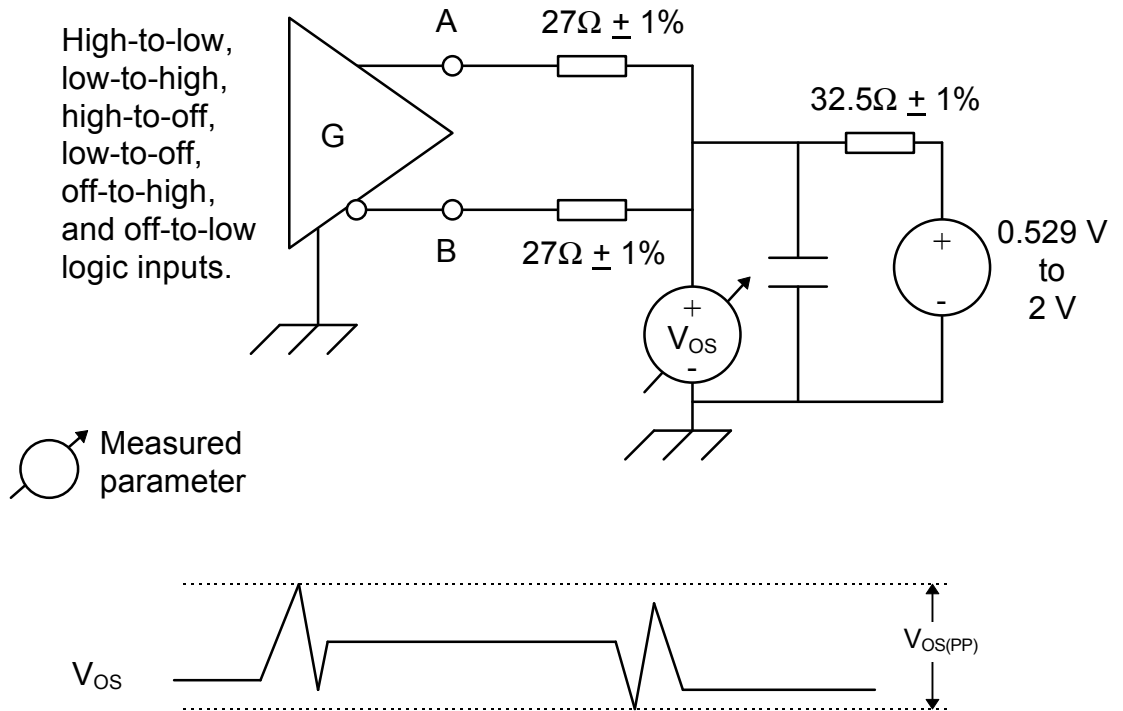


Figure 8 - Generator offset switching voltage test circuit.

1.2 Receiver characteristics

A receiver indicates the logical state of the LVD-SCSI bus as defined by the differential voltage that exists at the interchange. A difference voltage of 30 mV defines the state. The receiver must detect this difference over the allowable common-mode input voltage range as determined by the generator and terminator output offsets and ground difference voltages.

The requirements that follow, define these characteristics in terms of the voltages and currents defined in figure 9.

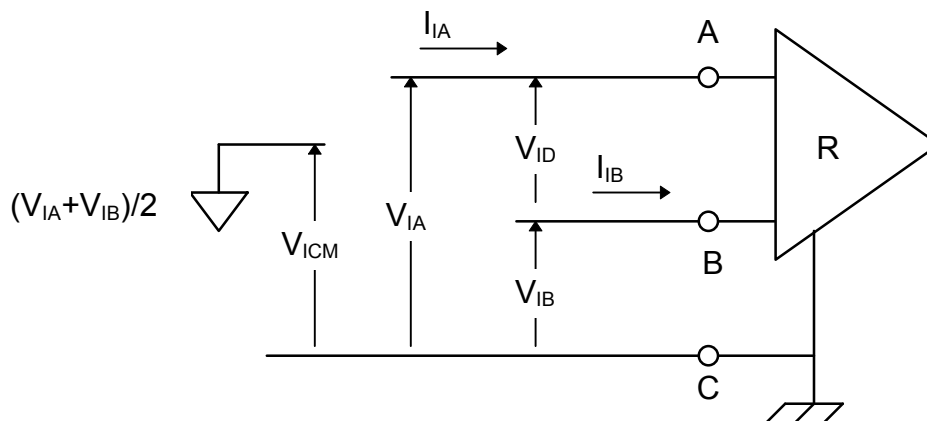


Figure 9 - Receiver voltage and current definitions.

1.2.1 Receiver input voltage threshold, V_{IT}

Within the common-mode input voltage range, a LVD-SCSI receiver shall not require a differential input voltage (V_{ID}) of more than ± 30 mV to correctly assume the intended binary

state. Reversing the polarity of V_{ID} shall cause the receiver to assume the opposite binary state.

$$V_{IT} < \pm 30 \text{ mV}$$

1.2.2 Receiver common-mode input voltage, V_{ICM}

A LVD-SCSI receiver shall meet its requirements over a common-mode input voltage range of 0.525 V to 2 V (referenced to receiver circuit common).

$$0.525 \text{ V} \leq V_{ICM} \leq 2 \text{ V}$$

1.2.3 Receiver differential input voltage, V_{ID}

The receiver shall indicate the logical state at the interchange with a differential input of up to 1050 mV.

$$-1.05 \text{ V} \leq V_{ID} \leq 1.05 \text{ V}$$

1.2.4 Receiver maximum input voltages

The receiver shall withstand a voltage at the A or B terminals not greater than 2.5 V or less than 0 V with respect to receiver circuit common without damage.

$$0 \text{ V} \leq V_{IA} \leq 2.5 \text{ V}$$

$$0 \text{ V} \leq V_{IB} \leq 2.5 \text{ V}$$

The receiver shall withstand a differential input voltage magnitude of 2.5 V and 1.25 V of common-mode input voltage with no damage occurring to the receiver inputs.

$$-2.5 \text{ V} \leq V_{ID} \leq 2.5 \text{ V}, \text{ with } V_{ICM} = 1.25 \text{ V}$$

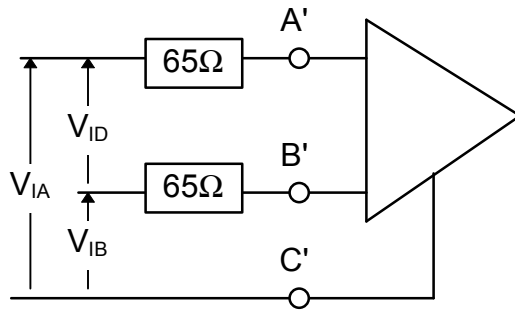
1.2.5 Compliance test

Compliance to the requirements above shall be verified with the input voltages of table 3 and the circuit of figure 10.

Table 3 - Receiver minimum and maximum input voltages.

Applied Voltages (Input Voltage - referenced to circuit common - C') (See figure 9)		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage
V_{IA}	V_{IB}	V_{ID}	V_{ICM}
0.54 V	0.51 V	0.03 V	0.525 V
0.51	0.54	-0.03	0.525
2.015	1.985	0.03	2
1.985	2.015	-0.03	2
1.05	0	1.05	0.525
0	1.05	-1.05	0.525
2.525	1.475	1.05	2
1.475	2.525	-1.05	2

Note: V_{IA} and V_{IB} voltages are ± 2 mV.



Resistors are 1% tolerance.

Figure 10 - Receiver input voltage threshold test circuit.

Note: The logic function of the receiver is not defined by this standard.

1.3 Generator/Receiver characteristics

1.3.1 Generator/receiver output/input currents, I_{IAL} and I_{IBL}

With the generator/receiver in an Off condition (i.e., not transmitting) and the output terminals short-circuited to a variable voltage source, the magnitudes of the currents (I_{IAL} and I_{IBL}) shall not exceed $20 \mu\text{A}$ over a test voltage range of 0 V to 2.5 V. (see figure 11)

These measurements apply with the generator/receiver's power supply in both power-on and power-off conditions.

$$|I_{IAL}| \leq 20 \mu\text{A}$$

$$|I_{IBL}| \leq 20 \mu\text{A}$$

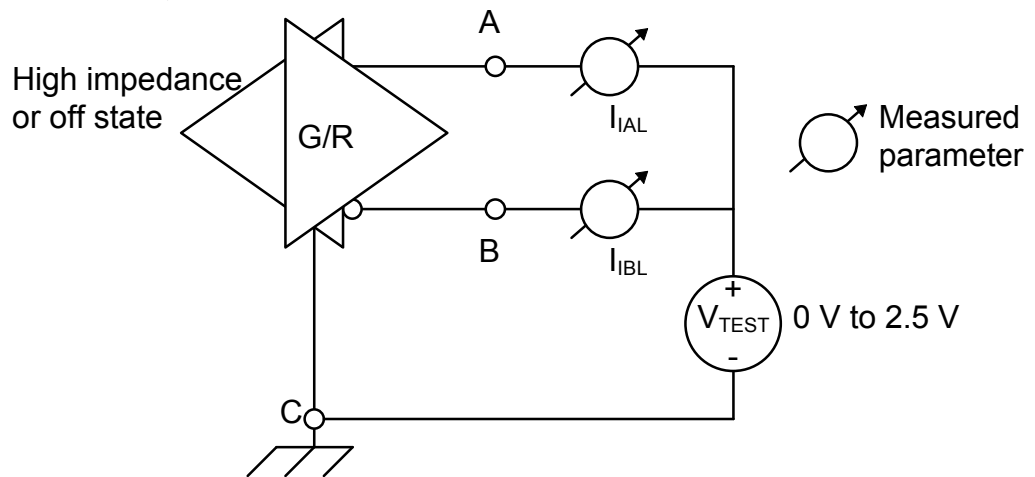


Figure 11 - Generator/receiver off-state output current test circuit.

1.3.2