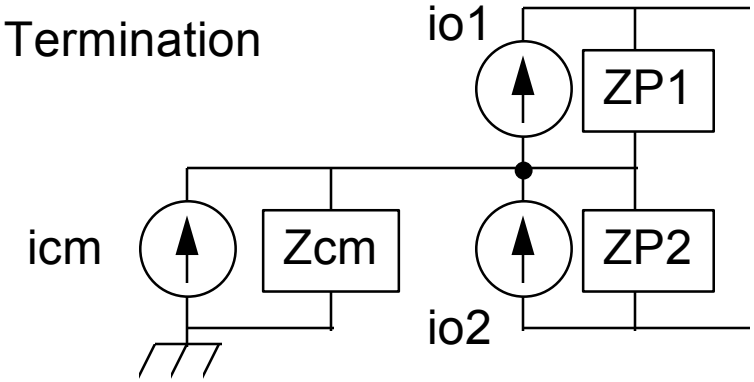
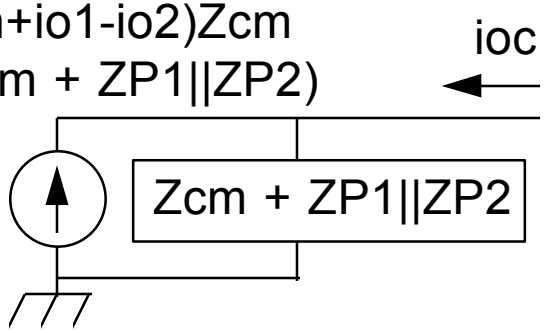
LVD SCSI Bus Components

Driver, Load, or Termination

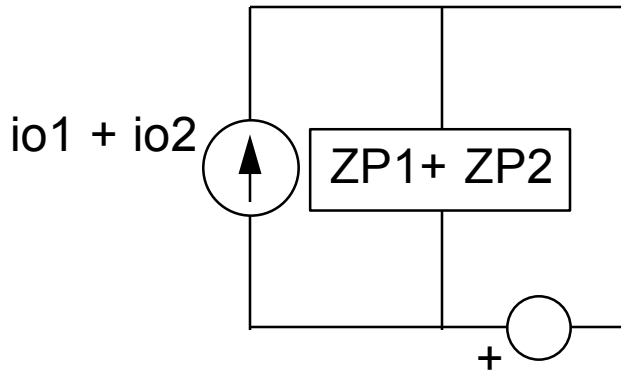


Common-mode

(icm+io1-io2)Zcm
/(Zcm + ZP1||ZP2)



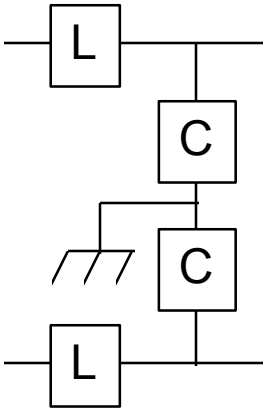
Differential



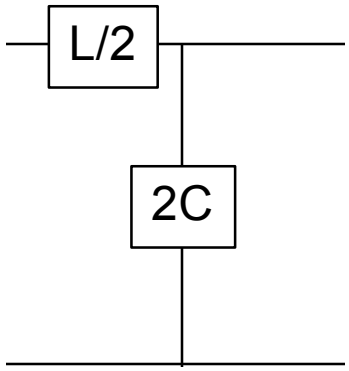
ioc(ZP1-ZP2)

LVD SCSI Bus Components

Lossless Media Segment

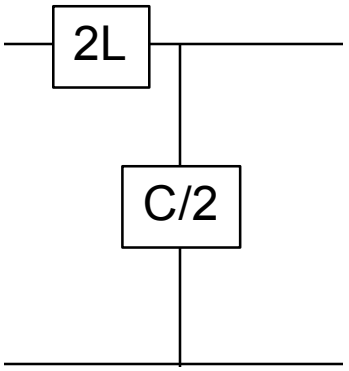


Common-mode



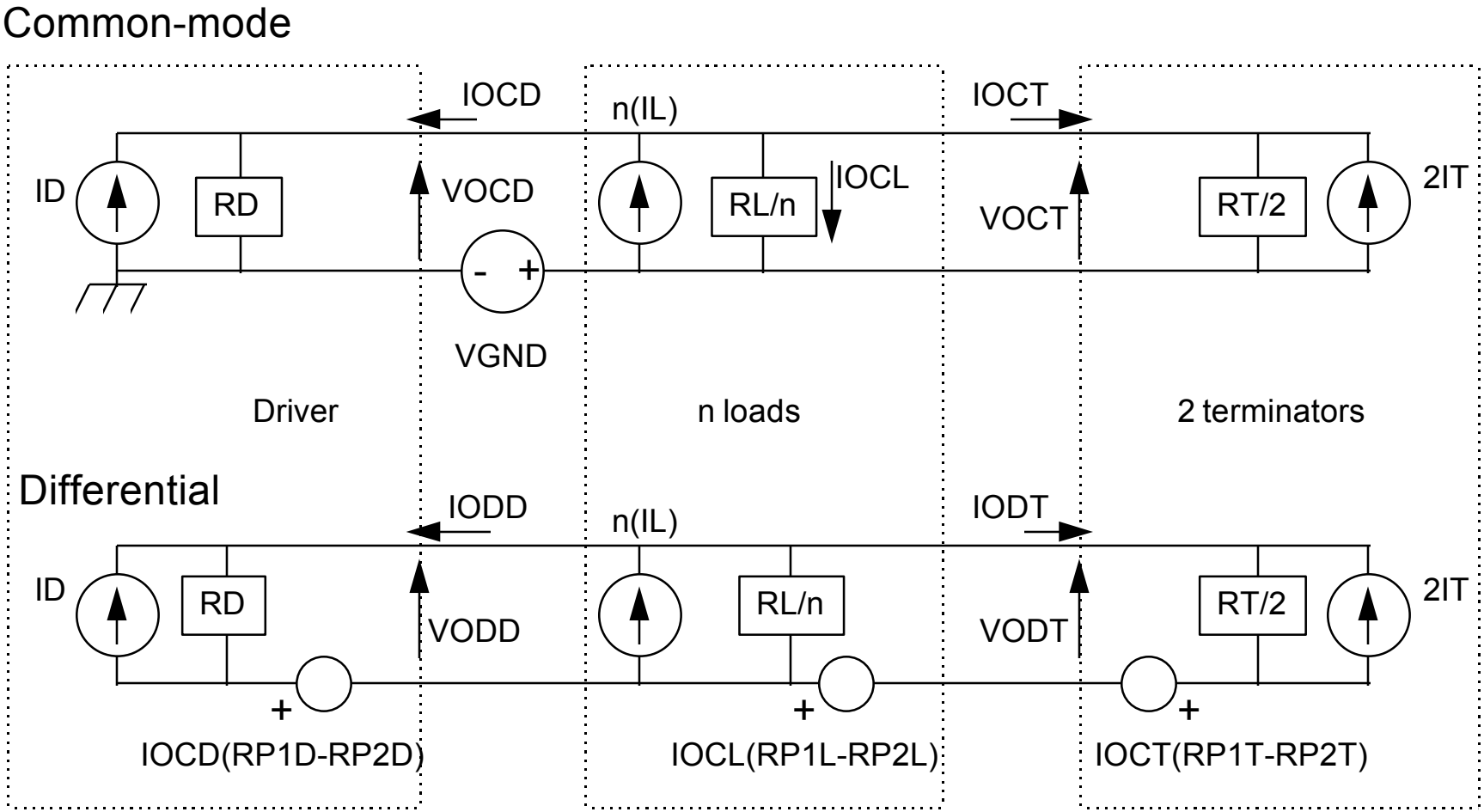
$$Z_{0cm} \approx \sqrt{\frac{L/2}{2C}}$$

Differential

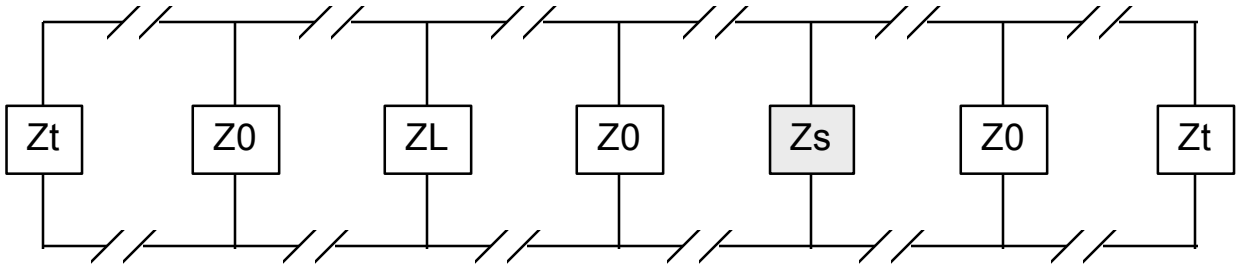


$$Z_{0d} \approx \sqrt{\frac{2L}{(C/2)}}$$

Bus DC Model


Common-mode
IOCD
n(IL)
IOCT
ID
RD
VOCD
RL/n
IOCL
VOCT
RT/2
2IT
- +
VGND
Driver
n loads
2 terminators
Differential
IODD
n(IL)
IODT
ID
RD
VODD
RL/n
VODT
RT/2
2IT
+
+
+
IOCD(RP1D-RP2D)
IOCL(RP1L-RP2L)
IOCT(RP1T-RP2T)

Bus AC Model



Common-mode

$$Z_t = Z_{CMt} + Z_{P1t} \| Z_{P2t}$$

$$Z_0 = \sqrt{\frac{L/2}{2C}}$$

$$Z_L = \sqrt{\frac{L/2}{\left(2C + \left(C_{i1} + C_{i2}\right)/d\right)}}$$

$$Z_S = Z_{CMd} + Z_{P1d} \| Z_{P2d}$$

Differential

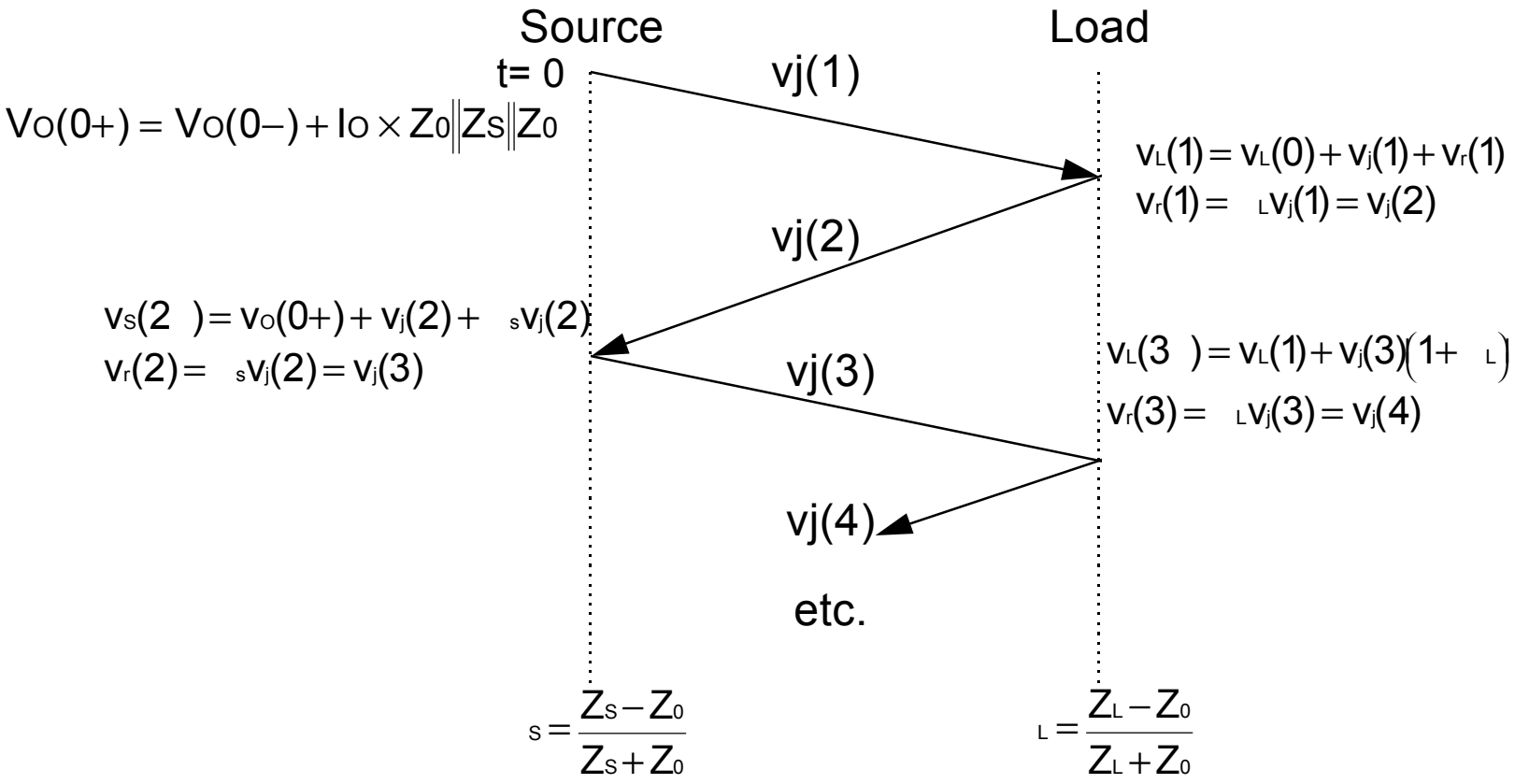
$$Z_t = Z_{P1t} + Z_{P2t}$$

$$Z_0 = \sqrt{\frac{2L}{(C/2)}}$$

$$Z_L = \sqrt{\frac{L}{\left(C/2 + \left(C_{i1}C_{i2}\right)/d\left(C_{i1} + C_{i2}\right)\right)}}$$

$$Z_S = Z_{P1d} + Z_{P2d}$$

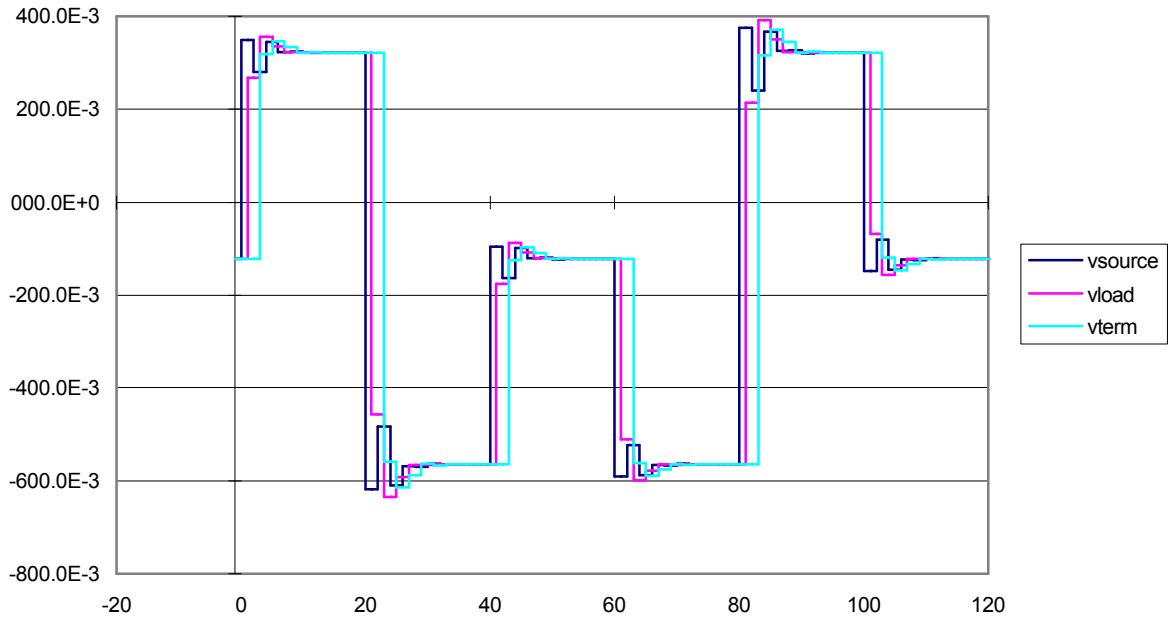
Lattice Diagram



Bus Signals

Nominal LVD-SCSI Differential

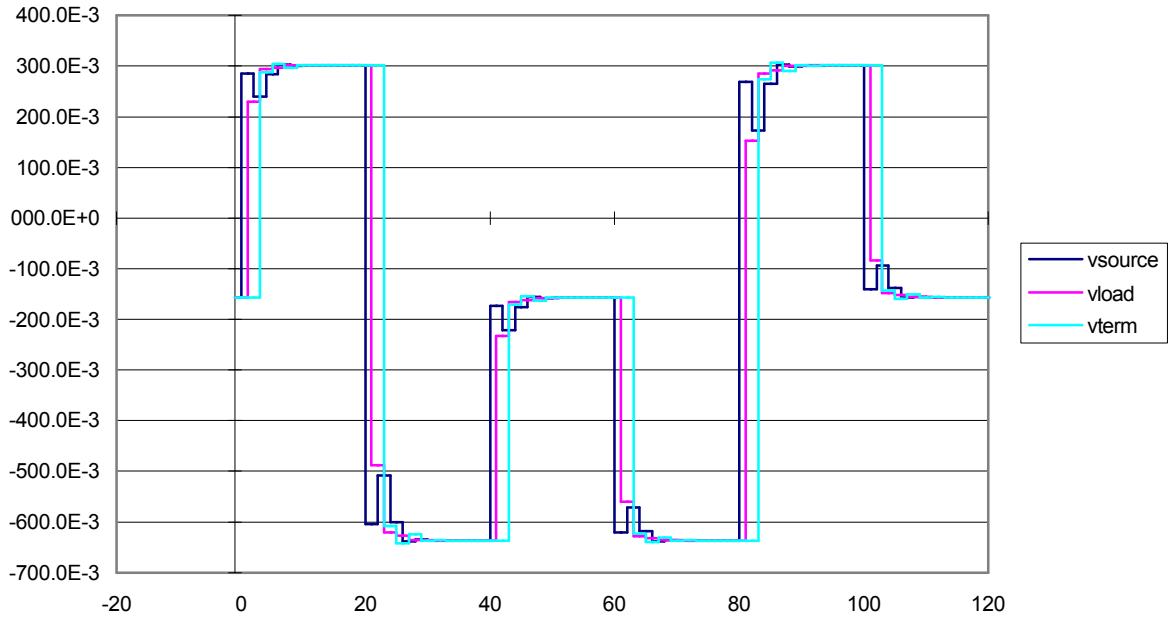
scenario	
0.12	vbias (open circuit)
120	z0
85	zload
9.3E-3	iout
112	zt
800E-9	iin
3.20E+02	rp
16	nodes
1	negation current multiplier
121.4E-3	vbias (loaded)
268.2E-3	passive-to-assertion min
-457.5E-3	assertion-to-negation min
-87E-3	negation-to-passive min
-599E-3	passive-to-negation min
215E-3	negation-to-assertion min
-68E-3	assertion-to-passive min
########	max negation voltage
########	max assertion voltage
23E-3	avg driver power



Bus Signals

Negation-to-Assertion Minimum

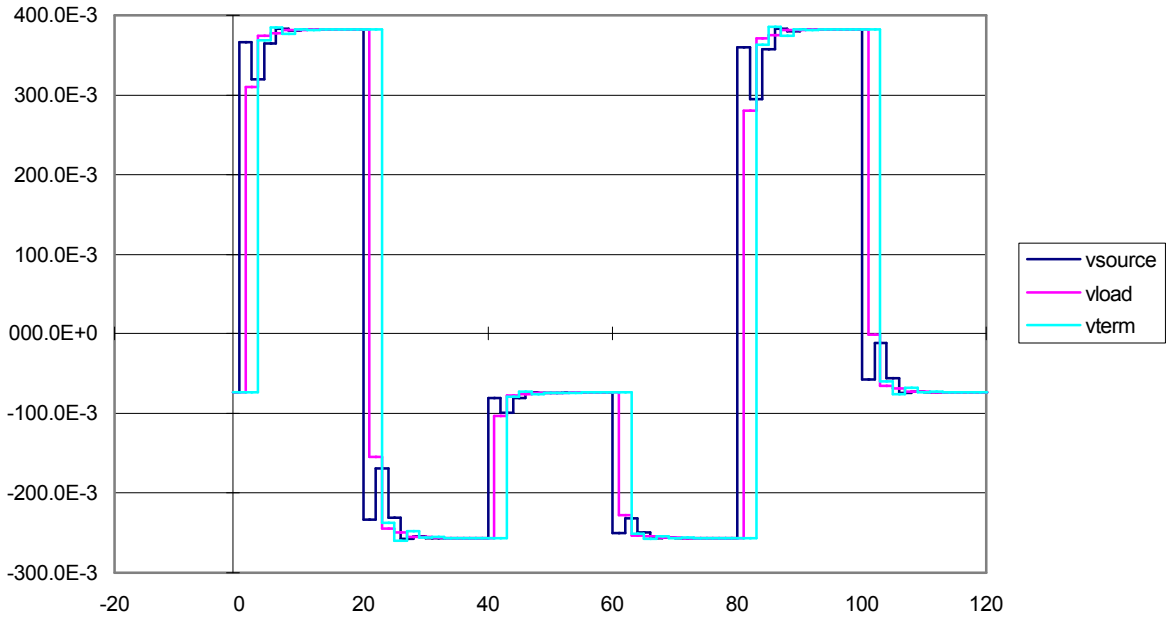
scenario	
0.13	vbias (open circuit)
110	z0
85	zload
9.8E-3	iout
115	zt
14E-6	iin
2.50E+02	rp
16	nodes
1.05	negation current multiplier
156.0E-3	vbias (loaded)
229.1E-3	passive-to-assertion min
-487.5E-3	assertion-to-negation min
-154E-3	negation-to-passive min
-640E-3	passive-to-negation min
153E-3	negation-to-assertion min
-83E-3	assertion-to-passive min
########	max negation voltage
########	max assertion voltage
23E-3	avg driver power



Bus Signals

Assertion-to-Negation Minimum

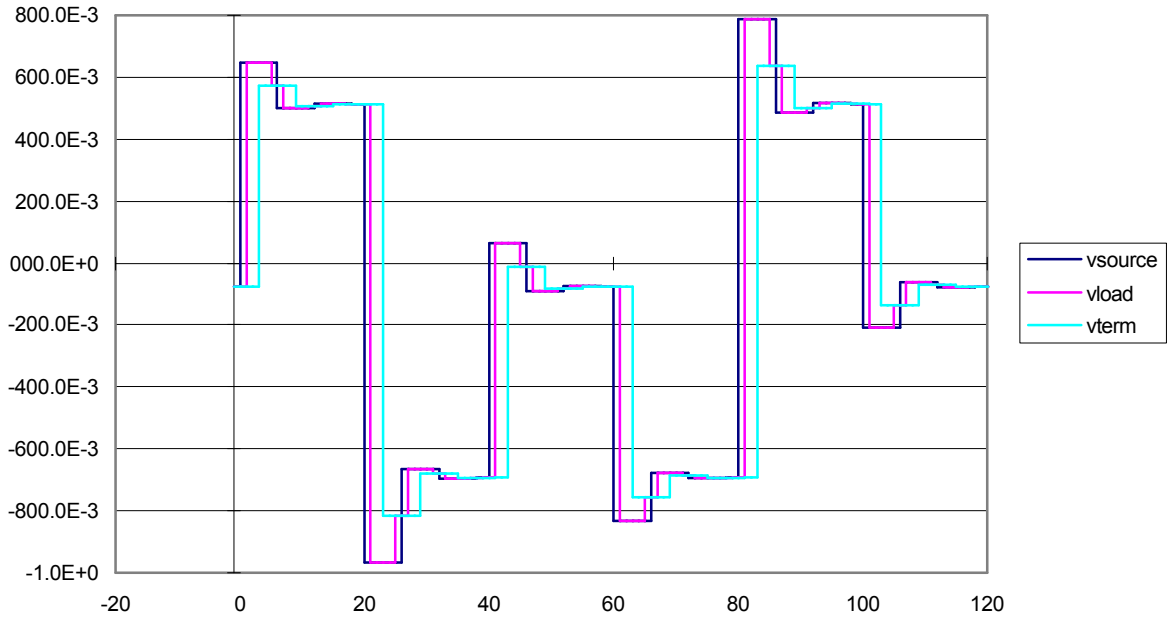
scenario	
0.1	vbias (open circuit)
110	z0
85	zload
9.8E-3	iout
115	zt
-14E-6	iin
2.50E+02	rp
16	nodes
0.4	negation current multiplier
74.0E-3	vbias (loaded)
309.7E-3	passive-to-assertion min
-154.8E-3	assertion-to-negation min
-73E-3	negation-to-passive min
-257E-3	passive-to-negation min
281E-3	negation-to-assertion min
-1E-3	assertion-to-passive min
#########	max negation voltage
#########	max assertion voltage
17E-3	avg driver power



Bus Signals

Negation-to-Passive Maximum

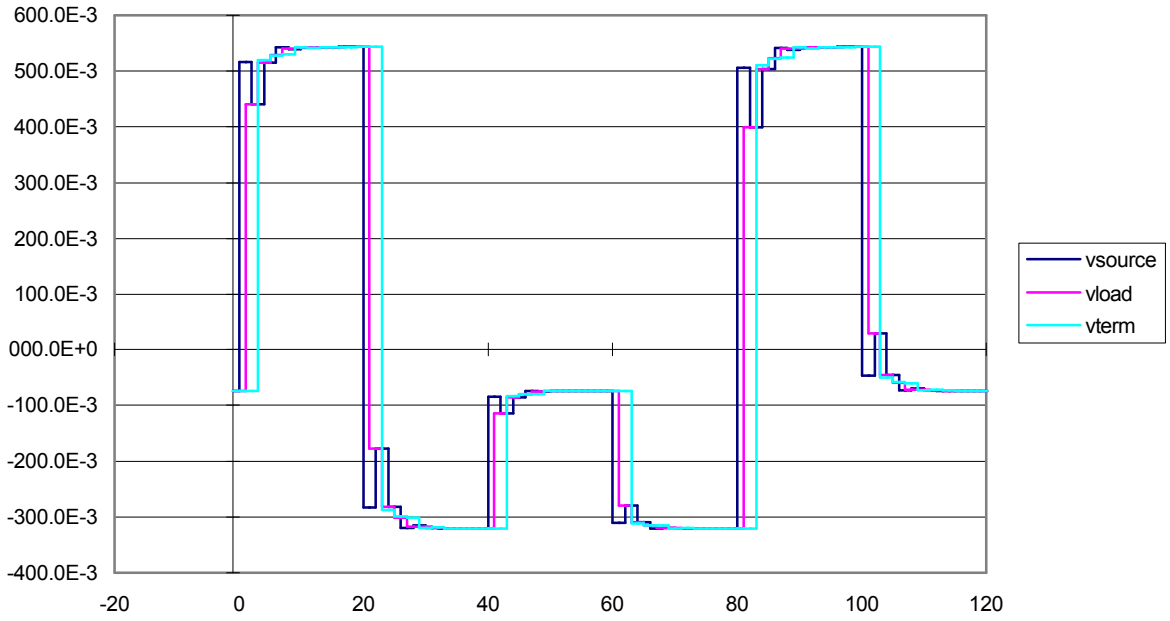
scenario	
0.1	vbias (open circuit)
135	z0
135	zload
10.7E-3	iout
110	zt
-14E-6	iin
1.00E+06	rp
16	nodes
1.05	negation current multiplier
75.1E-3	vbias (loaded)
499.7E-3	passive-to-assertion min
-665.0E-3	assertion-to-negation min
66E-3	negation-to-passive min
-834E-3	passive-to-negation min
485E-3	negation-to-assertion min
-61E-3	assertion-to-passive min
########	max negation voltage
########	max assertion voltage
29E-3	avg driver power



Bus Signals

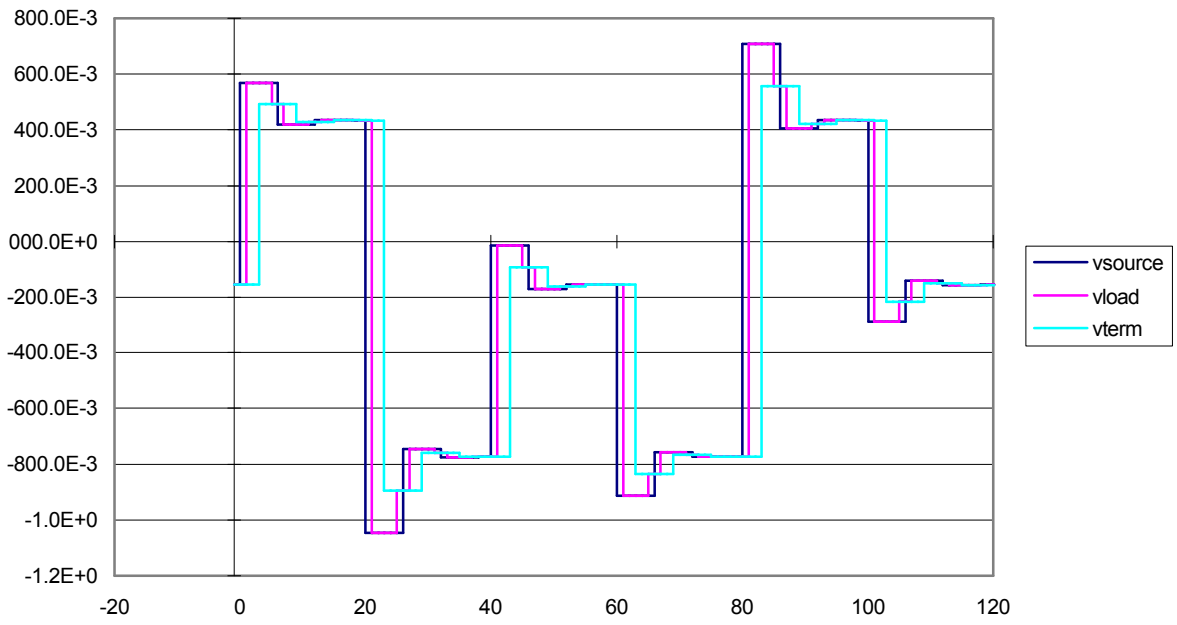
Assertion-to-Passive Maximum

scenario	
0.1	vbias (open circuit)
110	z0
85	zload
10.7E-3	iout
115	zt
-14E-6	iin
1.00E+06	rp
16	nodes
0.4	negation current multiplier
74.0E-3	vbias (loaded)
440.7E-3	passive-to-assertion min
-177.3E-3	assertion-to-negation min
-74E-3	negation-to-passive min
-321E-3	passive-to-negation min
400E-3	negation-to-assertion min
29E-3	assertion-to-passive min
########	max negation voltage
#########	max assertion voltage
22E-3	avg driver power



Bus Signals

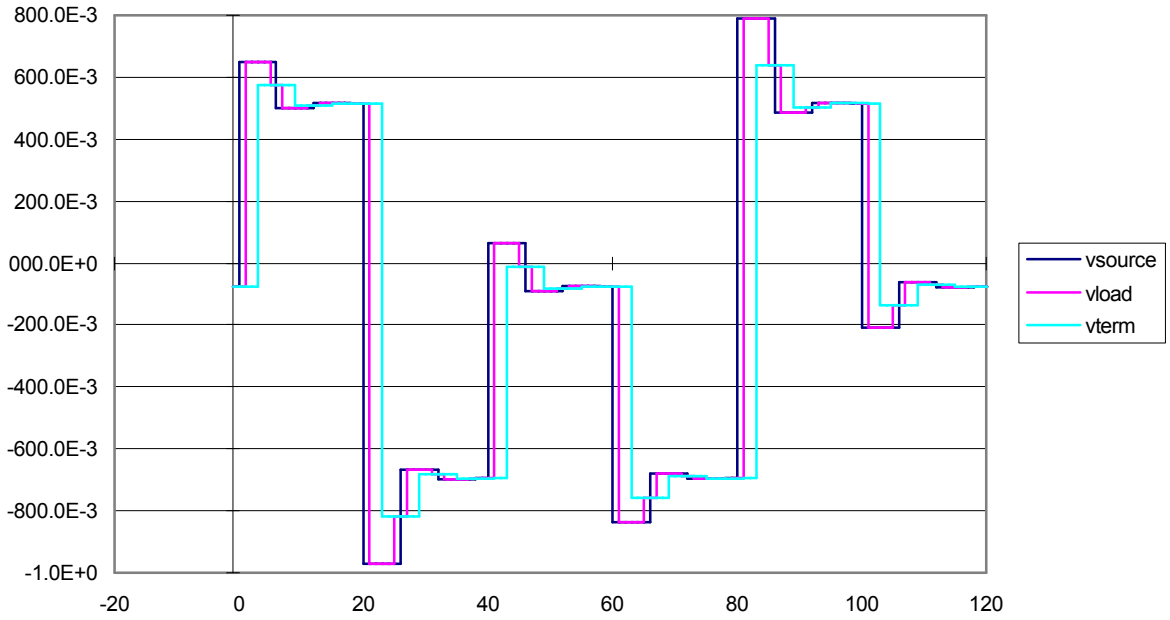
scenario	
0.13	vbias (open circuit)
135	z0
135	zload
10.7E-3	iout
110	zt
14E-6	iin
1.00E+06	rp
16	nodes
1.05	negation current multiplier
154.9E-3	vbias (loaded)
419.9E-3	passive-to-assertion min
-744.8E-3	assertion-to-negation min
-14E-3	negation-to-passive min
-913E-3	passive-to-negation min
406E-3	negation-to-assertion min
-141E-3	assertion-to-passive min
-1.05E+0	max negation voltage
#########	max assertion voltage
29E-3	avg driver power



Bus Signals

Maximum Assertion Voltage

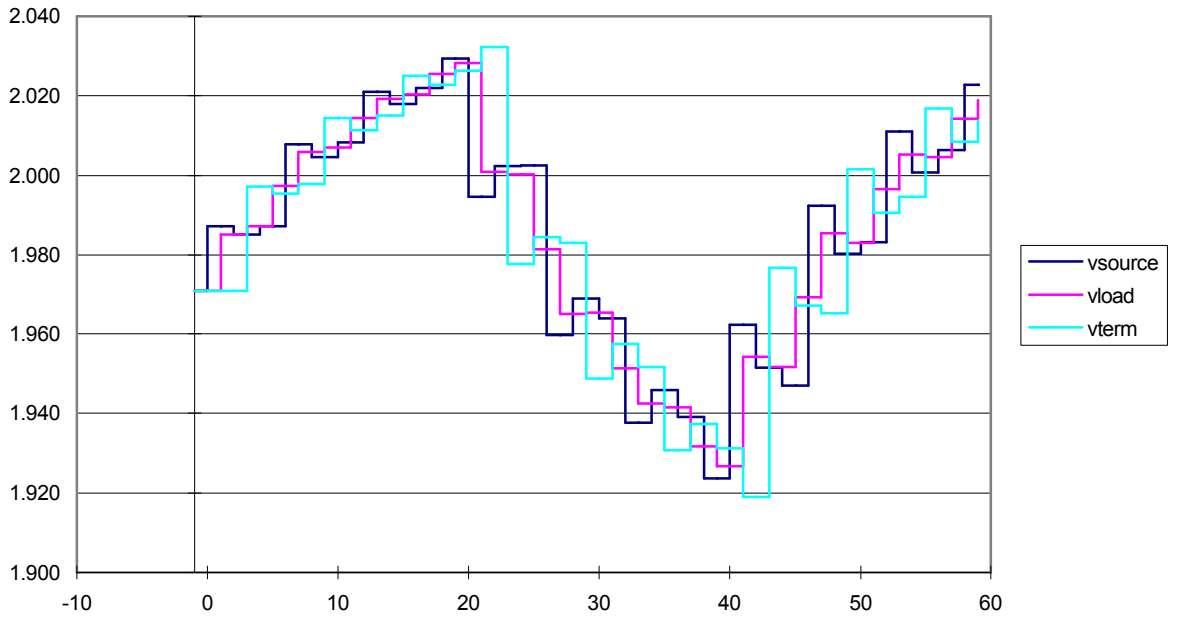
scenario	
0.1	vbias (open circuit)
135	z0
135	zload
10.7E-3	iout
110	zt
-14E-6	iin
1.00E+06	rp
16	nodes
1.05	negation current multiplier
75.1E-3	vbias (loaded)
501.6E-3	passive-to-assertion min
-667.0E-3	assertion-to-negation min
66E-3	negation-to-passive min
-836E-3	passive-to-negation min
487E-3	negation-to-assertion min
-61E-3	assertion-to-passive min
#########	max negation voltage
790E-3	max assertion voltage
29E-3	avg driver power



Bus Signals

Maximum Common-mode

scenario	
500E-6	icmd
1.375	vt(oc)
20E-6	iin
16	nodes
0.5	vgnd
65	z0
5.00E+05	zcmd
300	zcmt
50	zload
1.05	vodmax
1.971	vbias (loaded)
-4E-3	icmt
16.2E-3	vocd
2.6E+0	max voltage
1.4E+0	min voltage



Bus Signals

Minimum Common-mode Voltage

scenario	
500E-6	icmd
1.125	vt(oc)
-20E-6	iin
16	nodes
-0.5	vgnd
64.93506494	z0
5.00E+05	zcmd
300	zcmt
50	zload
1.05	vodmax
0.529	vbias (loaded)
4E-3	icmt
16.2E-3	vocd
1.1E+0	max voltage
-47.9E-3	min voltage