TERMINATOR RESISTOR MISMATCH PROBLEM

Richard Uber
6- Nov- 95
Quantum Corp.

NOMINAL COMPONENT VALUES:

\[\begin{array}{c}
\text{60} \\
+/- \\
| \\
\text{O} \\
| \\
\text{150} \\
\text{1.25v} \\
+/- \\
| \\
\text{O} \\
| \\
\text{60} \\
\text{60}
\end{array}\]

VOLTAGE SKEW CAUSED BY COMMON MODE OFFSETS AND RESISTOR TOLERANCES
- Minimum value for "150 ohm" common mode resistors
- Mismatched tolerences on "60 ohm" resistors
- +/- 0.5v ground offsets on terminators

\[\begin{array}{c}
\text{55 min} \\
+/- \\
| \\
\text{O} \\
| \\
\text{120} \\
\text{1.75v} \\
+/- \\
| \\
\text{O} \\
| \\
\text{65 max} \\
\text{55 min}
\end{array}\]

\[I_{\text{common mode}} = \frac{1.0v}{(120 + 120)/120 + 120 \text{ ohms}}\]
\[= \frac{1.0v}{300 \text{ ohms}} = 0.333mA\]

\[V_{\text{offset}} = (0.333mA/2 \times 65 \text{ ohms}) - (0.333mA/2 \times 55 \text{ ohms})\]
\[= 108.33mv - 91.66mv\]
\[= 16.67mv\]

This offset can be either polarity.

CONCLUSIONS:
1 A differential voltage offset of +/- 16.67mv is large relative to system noise margin of only 30mv.
2 On an individual terminator, the "60 ohm" resistors should match to within +/- 1-2% instead of the currently specified +/- 8.33%.
Nominal circuit for idle bus (all devices tristated) = NEGATION

\[
\begin{array}{c}
\text{Nominal circuit for idle bus (all devices tristated) = NEGATION} \\
60 & 60 \\
+/-/\//\//-/-/-/-/-/+ +/-/\//\//-/-/-/-/+ \\
+ | + \quad O 50-65mV | O 50-65mV \\
- | + \\
150 | \\
1.25v -/\//\//-/+ Voffset = 100-130mV +/-/-/-/\//\///+ \\
1.25v \\
+ | + \quad O 50-65mV | O 50-65mV \\
- | - \\
+/-/\//\//-/-/-/-/+ +/-/\//\//-/-/-/-/+ \\
60 & 60
\end{array}
\]

Driven Asserted

\[
\begin{array}{c}
\text{Driven Asserted} \\
60 & 60 \\
+/-/\//\//-/-/-/-/+ +/-/\//\//-/-/-/-/+ \\
+ | + \quad O 50-65mV | O 50-65mV \\
- | + \\
150 | \\
1.25v -/\//\//-/+ 430mV > Voffset > 400mV +/-/-/-/\//\///+ \\
1.25v \\
+ | + \quad O 50-65mV | O 50-65mV \\
- | - \\
+/-/\//\//-/-/-/-/+ +/-/\//\//-/-/-/-/+ \\
60 & 60 \\
\text{Driven Asserted} \\
60 & 60 \\
+/-/\//\//-/-/-/-/+ +/-/\//\//-/-/-/-/+ \\
+ | + \quad O 0-5mV | O 0-5mV \\
- | + \\
150 | \\
\end{array}
\]
If the bias generator is modeled as an ideal zener diode as shown in the draft specifications, then the following situation develops if there is a common mode voltage difference between the terminators due to ground offset.

Because current flows between terminators and not from driver pin to driver pin, the ideal bias generators split their directions. Half of them see "negation current" and half of them see "assertion current".

The result is that the passively negated bus sees only 50-70mV of bias instead of the 100mV required to insure proper operation of the LVDS receivers.

A better terminator model is required to enable LVDS protocol chip designers to do bus simulations.
ALTERNATE TERMINATOR MODEL SUITABLE FOR HSPICE

The HSpice VCR element can be defined as:

\[
\begin{align*}
R_{\text{var}} & \quad \text{min} \quad \text{max} \\
+10\text{mV} & < \text{V}_{\text{nn}} - \text{V}_{\text{pp}} & 10 \text{ ohms} & \quad 13 \text{ ohms} \\
\text{V}_{\text{nn}} - \text{V}_{\text{pp}} & < -10\text{mV} & 0.01 \text{ ohms} & \quad 1 \text{ ohm} \\
+10\text{mV} & > \text{V}_{\text{nn}} - \text{V}_{\text{pp}} & \text{linearly} & \text{linearly} \\
\text{varies from} & \text{varies from} & .01 \text{ to 10 ohms} & \quad 1 \text{ to 13 ohms}
\end{align*}
\]

ALTHOUGH THIS DIAGRAM USES "IDEAL HSPICE ELEMENTS" AND IS NOT PHYSICALLY REALIZABLE, IT DOES MIMIC THE TERMINATOR BEHAVIOR CLOSE ENOUGH TO ALLOW THE USER TO DO BUS SIMULATIONS.

Also note that there is zero time delay for the terminator to switch offset voltage. The Unitrode terminator proposal has an undefined delay time, but proposes capacitive bypass to allow waves to pass without delay.
ASSUMPTIONS:

- Receiver sensitivity = +/- 70mV
- Crosstalk for LVDS only bus = 35mV
- Terminator offset = 100 - 130mV favoring negation
  = 0 - 10mV when fighting an assertion
- Drive current is 4.4 - 6.0mA
- Terminator resistance = 110 - 130 ohms
- Line impedance = 120 - 160 ohms unloaded
- Loaded line impedance = TBD

Static cases:

<table>
<thead>
<tr>
<th>state1</th>
<th>state2</th>
<th>Rterm</th>
<th>Vterm</th>
<th>Zline</th>
<th>Idrvr</th>
<th>xtalk</th>
<th>V1</th>
<th>V2</th>
<th>Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negate</td>
<td>-</td>
<td>110</td>
<td>100mV</td>
<td>-</td>
<td>4.4mA</td>
<td>-</td>
<td>342mV</td>
<td>-</td>
<td>272mV</td>
</tr>
<tr>
<td>Assert</td>
<td>-</td>
<td>110</td>
<td>10mV</td>
<td>-</td>
<td>4.4mA</td>
<td>-</td>
<td>-232mV</td>
<td>-</td>
<td>162mV</td>
</tr>
<tr>
<td>Z=Negate</td>
<td>-</td>
<td>100mV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>100mV</td>
<td>-</td>
<td>30mV</td>
<td></td>
</tr>
</tbody>
</table>
FAST-40 NOISE MARGIN CASES
Incident wave transitions

DRIVEN NEGATION ---> HIGH IMPEDANCE NEGATION:

\[ V_1 = \text{Quiescent Negated voltage} \]
\[ V_{drv} = I \times R_{term}/2 \]
\[ V_{swing} = Z_{line} \times I_{max}/2 \]
\[ V_2 = V_1 - V_{swing} \]
\[ \text{Noise margin} = V_2 - (\text{rcvr sensitivity} + \text{crosstalk}) = V_2 - 70\text{mV} \]

Bus release transients, no crosstalk

<table>
<thead>
<tr>
<th>state1</th>
<th>state2</th>
<th>Rterm Vterm Zline I_{drv}</th>
<th>V1</th>
<th>V_{swing}</th>
<th>V2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negate</td>
<td>Negate</td>
<td>-120mV 100mV 160 6.0mA 430mV</td>
<td>-480mV</td>
<td>-50mV</td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>Negate</td>
<td>-90mV 100mV 150 6.0mA 430mV</td>
<td>-450mV</td>
<td>-20mV</td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>Negate</td>
<td>-60mV 100mV 140 6.0mA 430mV</td>
<td>-420mV</td>
<td>10mV</td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>Negate</td>
<td>-30mV 100mV 130 6.0mA 430mV</td>
<td>-390mV</td>
<td>40mV</td>
<td></td>
</tr>
<tr>
<td>Negate  Z=Negate 0mV</td>
<td>110</td>
<td>100mV</td>
<td>120</td>
<td>6.0mA</td>
<td>430mV</td>
</tr>
<tr>
<td>----------------------</td>
<td>-----</td>
<td>-------</td>
<td>-----</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>Negate  Z=Negate 30mV</td>
<td>110</td>
<td>100mV</td>
<td>110</td>
<td>6.0mA</td>
<td>430mV</td>
</tr>
<tr>
<td>Negate  Z=Negate 60mV</td>
<td>110</td>
<td>100mV</td>
<td>100</td>
<td>6.0mA</td>
<td>430mV</td>
</tr>
<tr>
<td>Negate  Z=Negate 90mV</td>
<td>110</td>
<td>100mV</td>
<td>90</td>
<td>6.0mA</td>
<td>430mV</td>
</tr>
</tbody>
</table>

**CONCLUSIONS:**

- Cable impedance needs to be limited to 110 ohms MAX.
- This is NOT compatible with current specification of 120 ohms MIN.
- We need to explore other alternatives.
ALTERNATIVES FOR BUS RELEASE TRANSITIONS

1 Ignore the state reversals
   - Causes serious problems with edge triggered signals REQ, ACK, RST.
   - Following synchronous data transfers, hardware which counts
     REQ pulses or ACK pulses may still be enabled.
   - Causes changes which would ripple far back into chip logic and
     into existing software.
   - Some vendors implement "bus monitors" which could detect and
     act on short assertions on any signal.
   - Not acceptable.

2 Turn off half of the driver at a time.
   - Would require creating an intermediate state for a bus round
     trip time.
   - Requires additional signal, timer in protocol chip core logic
   - Injects common mode signal onto bus.
   - Requires at least 2 steps to maintain noise margin.
   - Not acceptable.

3 Turn off driver in two steps.
   - Requires the ability to attenuate drive current to 40-60% of
     normal value.
   - Would require creating an intermediate state for a bus round
     trip time.
   - Requires additional signal, timer in protocol chip core logic
   - Does not inject common mode signal onto the bus.
   - Requires at least 2 steps to maintain noise margin.
   - Not acceptable.
4 Switch from driving current to driving voltage
- Lessens concern with mismatches between line impedance and termination impedance.
- Can be done internal to driver, without adding any capacitance to the SCSI pin.
- The target resistance value can be in a wide range, about 100-300 ohms.
- One implementation could be:

```
4.4-6.0mA
source
   v +------| M |------ (-) bus pin
   |       | U |------ (+) bus pin
   |       +-------| X |
   |       |       | / |
   |       |       |/ |
   |       +---------| M |
   |           | U |------ (+) bus pin
   |           +-------| X |
   | R /         |       | / |
   | /          |       / |
   | /          |       |
   | / <-       |       |
   | /          |       |
   | +-----------|       |
ATTENUATE    v
   |       |
circuit
   | 4.4-6.0mA
sink
```
FAST-40 NOISE MARGIN CASES
Incident wave transitions

ASSERTED --> DRIVEN NEGATED:

Incident wave negated voltage

\[
\begin{align*}
\text{noise margin} & : v \\
\text{crosstalk allowance} & : 105\text{mv} \\
\text{Rcvr sensitivity} & : 70\text{mv} \\
\text{Vdiff} & = 0 \\
\text{Vdrv} & = I \times \frac{\text{Rterm}}{2} \\
\text{Vswing} & = I \times \text{Zline} \\
\text{V1} & = (\min \text{ terminator offset}) + I_{\min} \times (\max \text{ terminator resistance})/2 \\
\text{Vswing} & = \text{Zline} \times I_{\min} / 2 \\
\text{V2} & = \text{V1} - \text{Vswing} \\
\text{Noise margin} & = \text{V2} - (\text{rcvr sensitivity} + \text{crosstalk}) = \text{V2} - 105\text{mv}
\end{align*}
\]

<table>
<thead>
<tr>
<th>state1</th>
<th>state2</th>
<th>Rterm</th>
<th>Vterm</th>
<th>Zline</th>
<th>Idrv</th>
<th>V1</th>
<th>Vswing</th>
<th>V2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assert</td>
<td>Negate</td>
<td>130</td>
<td>0mv</td>
<td>160</td>
<td>4.4ma</td>
<td>-286mv</td>
<td></td>
<td></td>
</tr>
<tr>
<td>704mv</td>
<td>418mv</td>
<td>313mv</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assert</td>
<td>Negate</td>
<td>130</td>
<td>0mv</td>
<td>140</td>
<td>4.4ma</td>
<td>-286mv</td>
<td></td>
<td></td>
</tr>
<tr>
<td>616mv</td>
<td>330mv</td>
<td>225mv</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assert</td>
<td>Negate</td>
<td>130</td>
<td>0mv</td>
<td>120nom</td>
<td>4.4ma</td>
<td>-286nom</td>
<td></td>
<td></td>
</tr>
<tr>
<td>528mv</td>
<td>242mv</td>
<td>137mv</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assert</td>
<td>Negate</td>
<td>130</td>
<td>0mv</td>
<td>110</td>
<td>4.4ma</td>
<td>-286mv</td>
<td></td>
<td></td>
</tr>
<tr>
<td>198mv</td>
<td>93mv</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assert</td>
<td>Negate</td>
<td>130</td>
<td>0mv</td>
<td>100</td>
<td>4.4ma</td>
<td>-286mv</td>
<td></td>
<td></td>
</tr>
<tr>
<td>154mv</td>
<td>49mv</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assert</td>
<td>Negate</td>
<td>130</td>
<td>0mV</td>
<td>90</td>
<td>4.4mA</td>
<td>-286mV</td>
<td>396mV</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>--------</td>
<td>-----</td>
<td>-----</td>
<td>----</td>
<td>--------</td>
<td>---------</td>
<td>-------</td>
<td></td>
</tr>
<tr>
<td>110mV</td>
<td>5mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
FAST-40 NOISE MARGIN CASES
Incident wave transitions

DRIVEN NEGATED --> ASSERTED:

\[ V_{	ext{diff}} = 0 \]

\[ V_1 = (\text{min terminator offset}) + I_{\text{min}} \times (\text{max terminator resistance})/2 \]

\[ V_{\text{swing}} = Z_{\text{line}} \times I_{\text{min}} / 2 \]

\[ V_2 = V_1 - V_{\text{swing}} \]

\[ \text{Noise margin} = V_2 - (\text{rcvr sensitivity} + \text{crosstalk}) = |V_2 - (-105\text{mV})| \]

<table>
<thead>
<tr>
<th>state1</th>
<th>state2</th>
<th>Rterm</th>
<th>Vterm</th>
<th>Zline</th>
<th>Idvr</th>
<th>V1</th>
<th>Vswing</th>
<th>V2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negate</td>
<td>Assert</td>
<td>130</td>
<td>130mV</td>
<td>160</td>
<td>4.4mA</td>
<td>416mV</td>
<td>-704mV</td>
<td>-288mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>130mV</td>
<td>183mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>Assert</td>
<td>130</td>
<td>130mV</td>
<td>140</td>
<td>4.4mA</td>
<td>416mV</td>
<td>-616mV</td>
<td>-200mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>130mV</td>
<td>95mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>Assert</td>
<td>130</td>
<td>130mV</td>
<td>120</td>
<td>4.4mA</td>
<td>416mV</td>
<td>-528mV</td>
<td>-112mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>130mV</td>
<td>7mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>Assert</td>
<td>130</td>
<td>130mV</td>
<td>110</td>
<td>4.4mA</td>
<td>416mV</td>
<td>-484mV</td>
<td>-68mV</td>
</tr>
<tr>
<td>Negate</td>
<td>Assert</td>
<td>130</td>
<td>130mV</td>
<td>100</td>
<td>4.4mA</td>
<td>416mV</td>
<td>-440mV</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>--------</td>
<td>-----</td>
<td>-------</td>
<td>-----</td>
<td>-------</td>
<td>-------</td>
<td>--------</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-24mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-81mV</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Negate</th>
<th>Assert</th>
<th>130</th>
<th>130mV</th>
<th>90</th>
<th>4.4mA</th>
<th>416mV</th>
<th>-396mV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>20mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-125mV</td>
</tr>
</tbody>
</table>

Trying larger minimum drive currents:

<table>
<thead>
<tr>
<th>Negate</th>
<th>Assert</th>
<th>130</th>
<th>130mV</th>
<th>100</th>
<th>5.0mA</th>
<th>425mV</th>
<th>-500mV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-50mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-55mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Negate</th>
<th>Assert</th>
<th>130</th>
<th>130mV</th>
<th>100</th>
<th>6.0mA</th>
<th>490mV</th>
<th>-600mV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-110mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Negate</th>
<th>Assert</th>
<th>130</th>
<th>130mV</th>
<th>100</th>
<th>7.0mA</th>
<th>555mV</th>
<th>-700mV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-145mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>40mV</td>
</tr>
</tbody>
</table>

Trying lower termination resistances (45-55 ohms):

<table>
<thead>
<tr>
<th>Negate</th>
<th>Assert</th>
<th>110</th>
<th>130mV</th>
<th>100</th>
<th>5.0mA</th>
<th>375mV</th>
<th>-500mV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-125mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>20mV</td>
</tr>
</tbody>
</table>
RECOMMENDATIONS

- Add a new state to be transitioned through when disconnecting from the bus. Connect a resistance between the positive and negative current sources. This resistance is in parallel with the transmission line, and will permit the SCSI device to exit from the LVDS bus without any assertion glitches.

- Consider lowering the termination resistance from 60 +/- 5 ohms to 50 +/- 3 ohms.

- Specify tighter matching for differential mode resistors within a terminator chip.

- Raise drive current range from 4.4 - 6.0 mA to 5.0 - 7.0 mA

- Limit loaded line impedance to 100 ohms minimum