TERMINATOR RESISTOR MISMATCH PROBLEM:

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6-NOV-95
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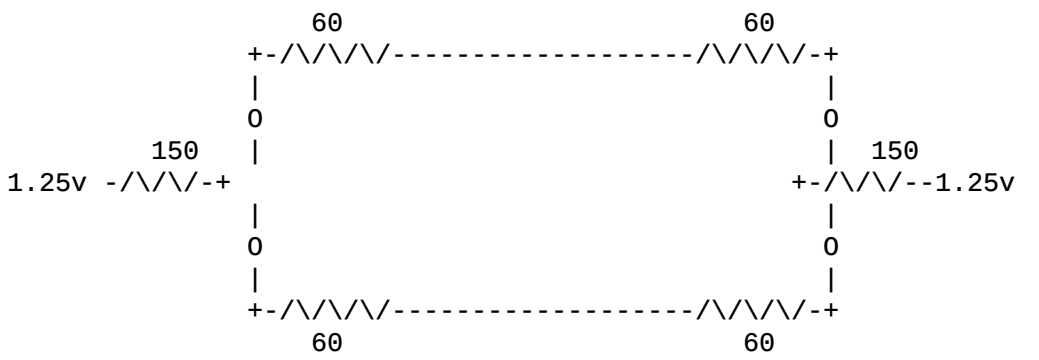
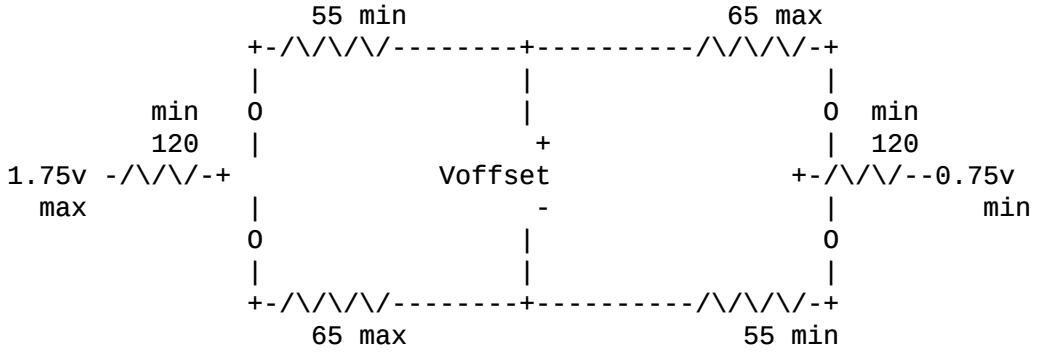
NOMINAL COMPONENT VALUES:



VOLTAGE SKEW CAUSED BY COMMON MODE OFFSETS AND RESISTOR TOLERANCES
- minimum value for "150 ohm" common mode resistors
- mismatched tolerences on "60 ohm" resistors
- +/- 0.5v ground offsets on terminators



Icommon mode = 1.0v / (120 + 120//120 + 120 ohms)
= 1.0v / 300 ohms = 0.333mA

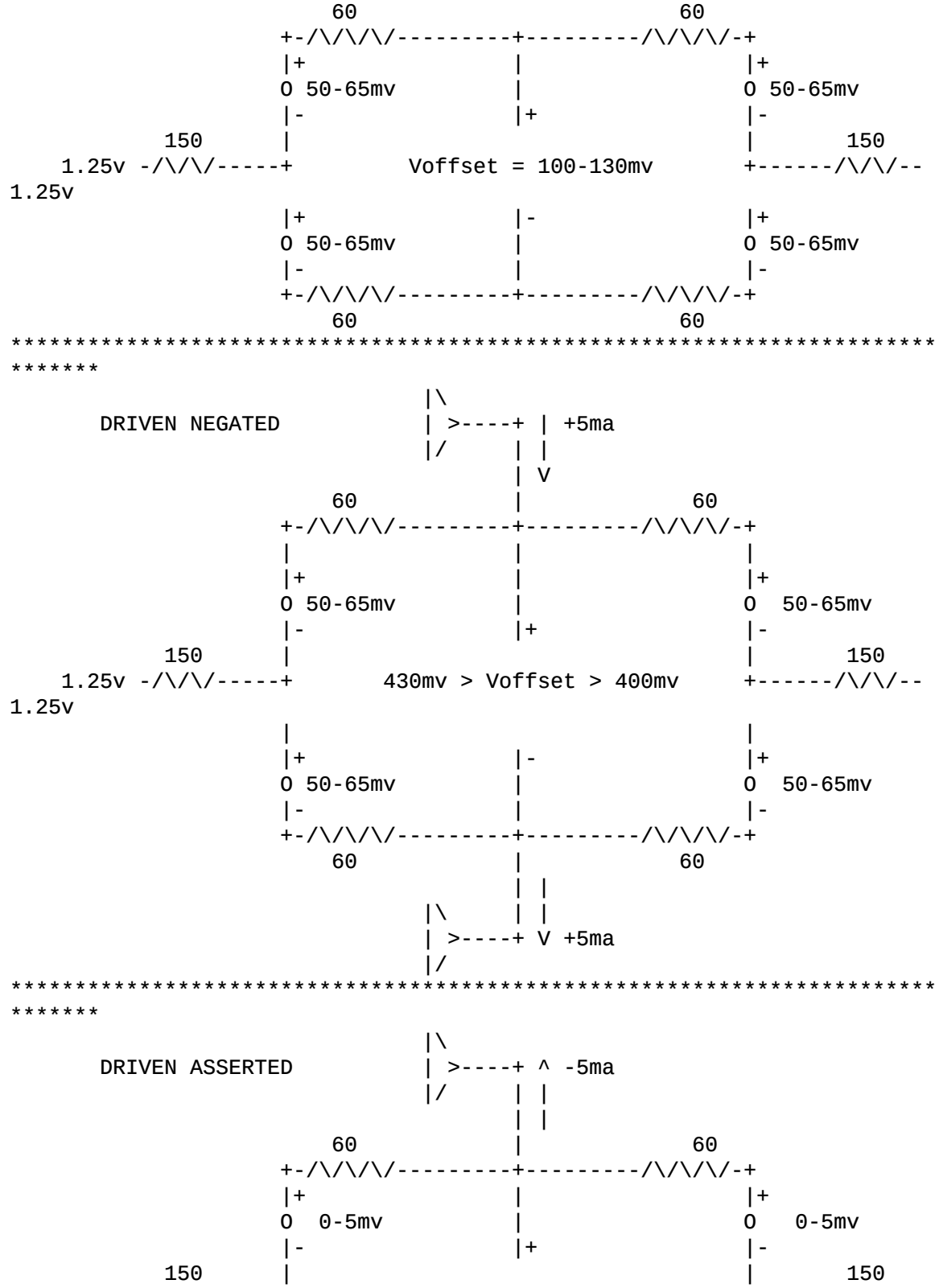
Voffset = (0.333ma/2 * 65 ohms) - (0.333ma/2 * 55 ohms)
= 108.33mv - 91.66mv
= 16.67mv
This offset can be either polarity.

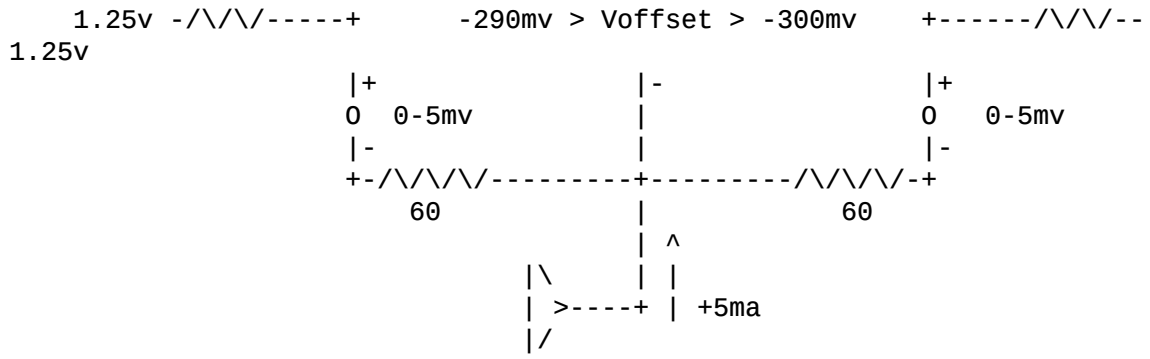
CONCLUSIONS:

1 A differential voltage offset of +/- 16.67mv is large relative to system noise margin of only 30mv.

2 On an individual terminator, the "60 ohm" resistors should match to within +/- 1-2% instead of the currently specified +/- 8.33%.

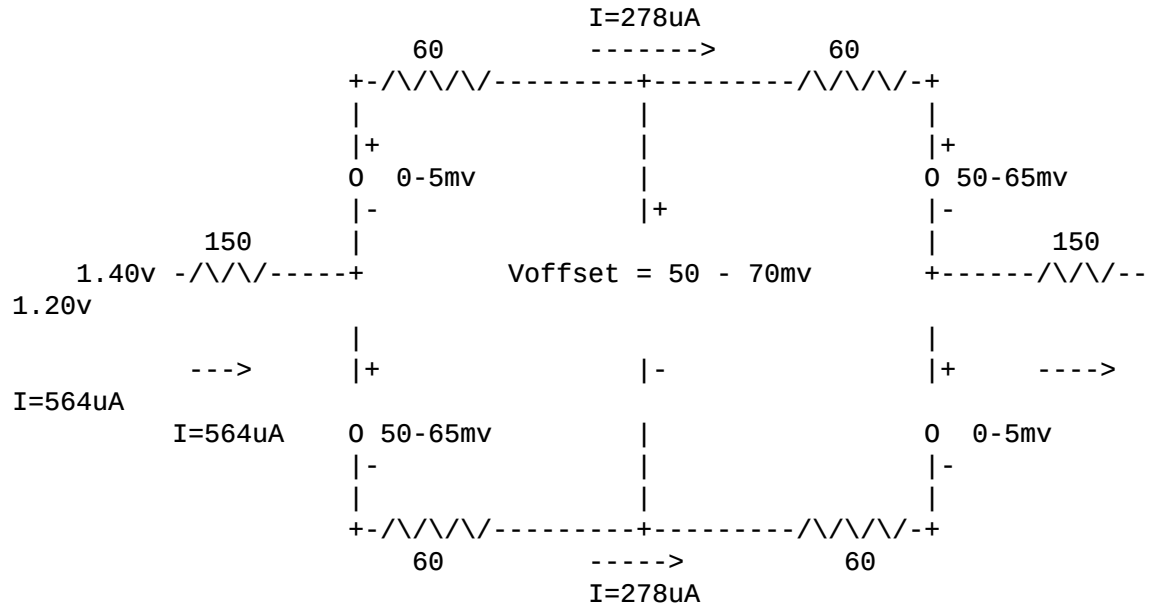
Nominal circuit for idle bus (all devices tristated) = NEGATION




1.25v -/\/\/-----+
-290mv > Voffset > -300mv
+------/\/\/--
1.25v
|+
O 0-5mv
|-
|-
|
|+
O 0-5mv
|-
+-/\/\/\/---------+---------/\/\/\/-+
60
|
60
| ^
|\
| |
| >----+ | +5ma
|/

TERMINATOR MODEL PROBLEM

If the bias generator is modeled as an ideal zener diode as shown in the draft specifications, then the following situation develops if there is a common mode voltage difference between the terminators due to ground offset.

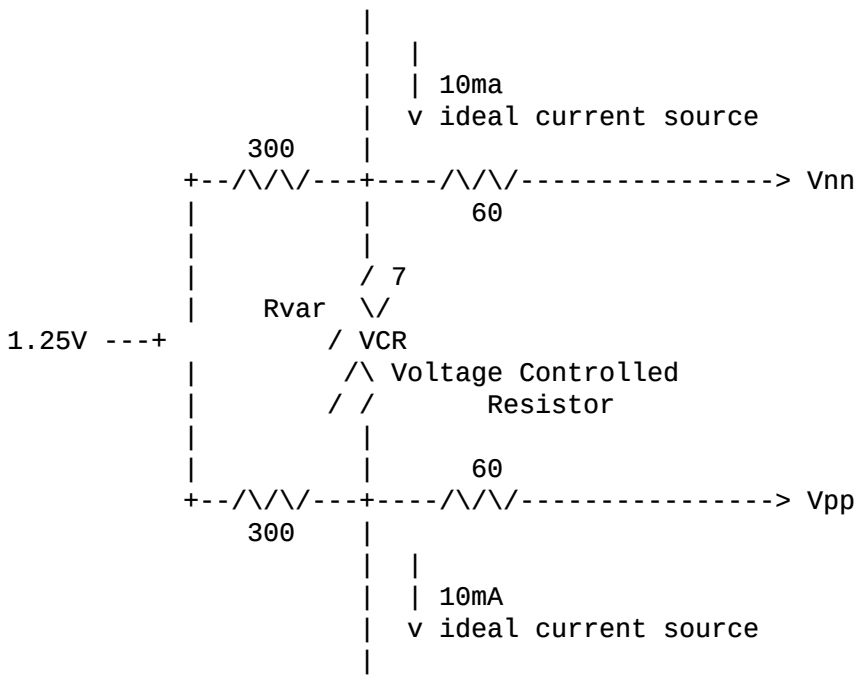


Because current flows between terminators and not from driver pin to driver pin, the ideal bias generators split their directions. Half of them see "negation current" and half of them see "asertion current".

THE RESULT IS THAT THE PASSIVELY NEGATED BUS SEES ONLY 50-70MV OF BIAS INSTEAD OF THE 100MV REQUIRED TO INSURE PROPER OPERATION OF THE LVDS RECEIVERS.

A BETTER TERMINATOR MODEL IS REQUIRED TO ENABLE LVDS PROTOCOL CHIP DESIGNERS TO DO BUS SIMULATIONS.

ALTERNATE TERMINATOR MODEL SUITABLE FOR HSPICE



The HSpice VCR element can be defined as:

	Rvar min	Rvar max
+10mv < Vnn - Vpp	10 ohms	13 ohms
Vnn - Vpp < -10mv	0.01 ohms	1 ohm
+10mv > Vnn - Vpp > -10mv	linearly varies from .01 to 10 ohms	linearly varies from 1 to 13 ohms

ALTHOUGH THIS DIAGRAM USES "IDEAL HSPICE ELEMENTS" AND IS NOT PHYSICALLY REALIZABLE, IT DOES MIMIC THE TERMINATOR BEHAVIOR CLOSE ENOUGH TO ALLOW THE USER TO DO BUS SIMULATIONS.

Also note that there is zero time delay for the terminator to switch offfset voltage. The Unitrode terminator proposal has an undefined delay time, but proposes capacitive bypass to allow waves to pass without delay.

FAST-40 NOISE MARGIN

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ASSUMPTIONS:

- Receiver sensitivity = +/- 70mv

- Crosstalk for LVDS only bus = 35mv

- Terminator offset = 100 - 130mv favoring negation
  = 0 - 10mv when fighting an assertion

- Drive current is 4.4 - 6.0mA

- Terminator resistance = 110 - 130 ohms

- Line impedence = 120 - 160 ohms unloaded

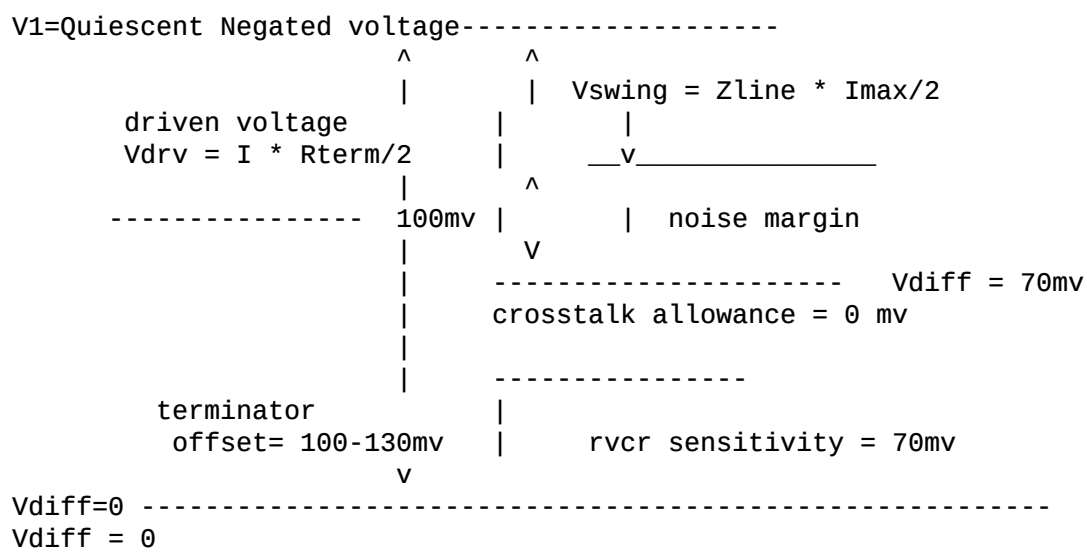
- Loaded line impedence = TBD

Static cases:

state1		state2		Rterm		Vterm		Zline	Idrvr		xtalk		V1		V2		Margin
Negate	-	110		100mv	-			4.4ma	-		342mv	-					272mv
Assert	-	110		10mv	-			4.4ma	-		-232mv	-					162mv
Z=Negate	-	-		100mv	-		-	-		100mv		-			30mv		

FAST-40 NOISE MARGIN CASES
Incident wave transitions

DRIVEN NEGATION ---> HIGH IMPEDENCE NEGATION:



V1 = (min terminator offset) + Imax * (min terminator resistance)/2

Vswing = Zline * Imax / 2

V2 = V1 - Vswing

Noise margin = V2 - (rcvr sensitivity + crosstalk) = V2 - 70mv

Bus release transients, no crosstalk

state1	state2	Rterm	Vterm	Zline	Idrvr	V1	Vswing	V2	Margin
Negate	Z=Negate	110	100mv	160	6.0ma	430mv	-480mv	-50mv	-120mv
Negate	Z=Negate	110	100mv	150	6.0ma	430mv	-450mv	-20mv	-90mv
Negate	Z=Negate	110	100mv	140	6.0ma	430mv	-420mv	10mv	-60mv
Negate	Z=Negate	110	100mv	130	6.0ma	430mv	-390mv	40mv	-30mv

Negate Z=Negate 0mv	110	100mv	120	6.0ma	430mv	-360mv	70mv
Negate Z=Negate 30mv	110	100mv	110	6.0ma	430mv	-330mv	100mv
Negate Z=Negate 60mv	110	100mv	100	6.0ma	430mv	-300mv	130mv
Negate Z=Negate 90mv	110	100mv	90	6.0ma	430mv	-270mv	160mv

CONCLUSIONS:

- Cable impedence needs to be limited to 110 ohms MAX.

- This is NOT compatible with current specification of 120 ohms MIN.

- We need to explore other alternatives.

ALTERNATIVES FOR BUS RELEASE TRANSITIONS

1 Ignore the state reversals
- Causes serious problems with edge triggered signals REQ, ACK, RST.
- Following synchronous data transfers, hardware which counts REQ pulses or ACK pulses may still be enabled.
- Causes changes which would ripple far back into chip logic and into existing software.
- Some vendors implement "bus monitors" which could detect and act on short assertions on any signal.
- Not acceptable.

2 Turn off half of the driver at a time.
- Would require creating an intermediate state for a bus round trip time.

state	pin--	pin++
driven negation	+5mA	-5ma
intermediate mode	+5ma	Z
passive negation	Z	Z

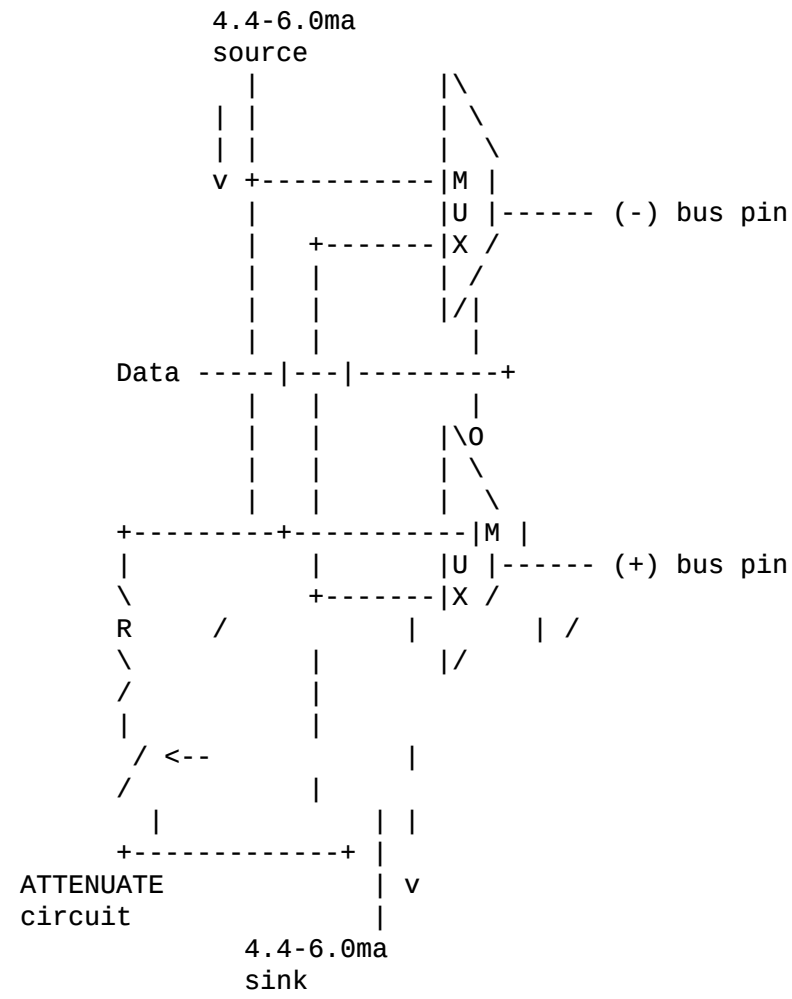
- Requires additional signal, timer in protocol chip core logic
- Injects common mode signal onto bus.
- Requires at least 2 steps to maintain noise margin.
- Not acceptable.

3 Turn off driver in two steps.
- Requires the ability to attenuate drive current to 40-60% of normal value.
- Would require creating an intermediate state for a bus round trip time.

state	pin--	pin++
driven negation	+5mA	-5ma
intermediate mode	+2 -> +3ma	-2 -> -3ma
passive negation	Z	Z

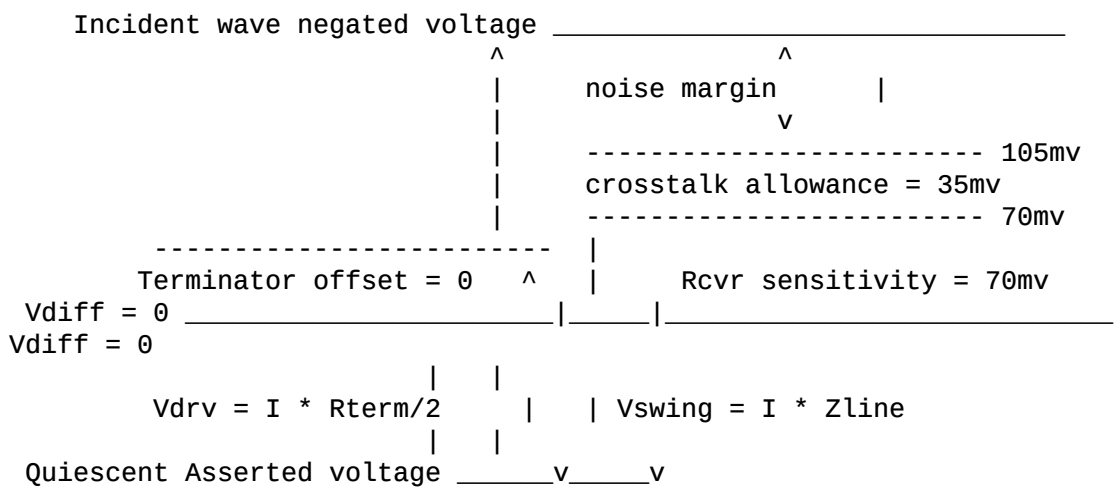
- Requires additional signal, timer in protocol chip core logic
- Does not inject common mode signal onto the bus.
- Requires at least 2 steps to maintain noise margin.
- Not acceptable.

4 Switch from driving current to driving voltage
- Lessens concern with mismatches between line impedance and termination impedance.
- Can be done internal to driver, without adding any capacitance to the SCSI pin.
- The target resistance value can be in a wide range, about 100-300 ohms.
- One implementation could be:



FAST-40 NOISE MARGIN CASES
Incident wave transitions

ASSERTED --> DRIVEN NEGATED:



V1 = (min terminator offset) + Imin * (max terminator resistance)/2

Vswing = Zline * Imin / 2

V2 = V1 - Vswing

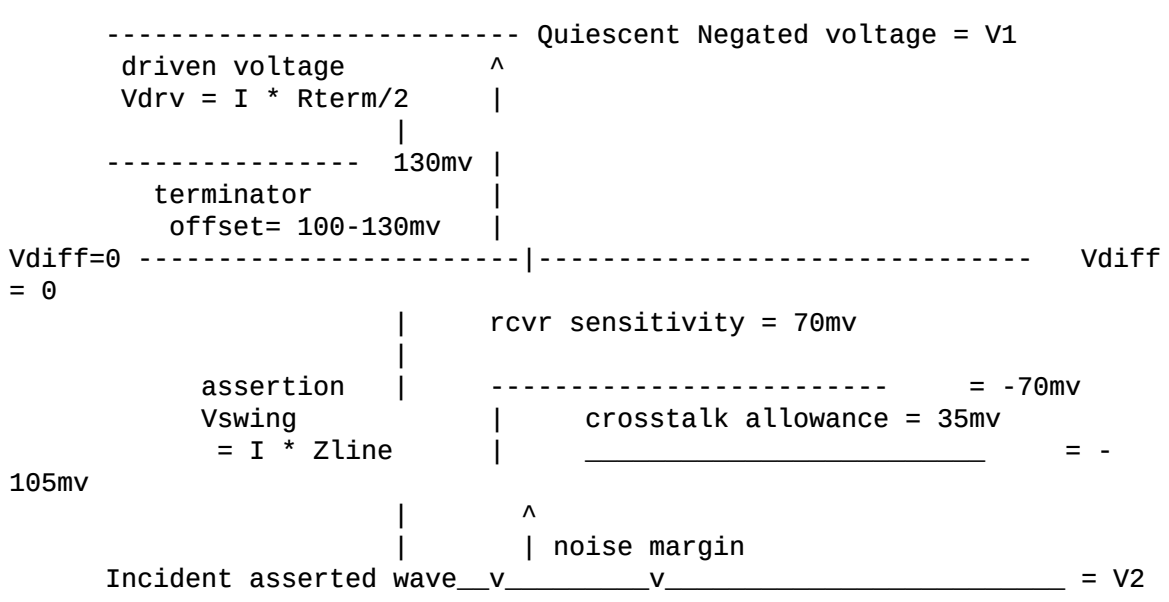
Noise margin = V2 - (rcvr sensitivity + crosstalk) = V2 - 105mv

state1	state2	Rterm	Vterm	Zline	Idrvr	V1	Vswing	V2	Margin
Assert	Negate	130	0mv	160	4.4ma	-286mv	704mv	418mv	313mv
Assert	Negate	130	0mv	140	4.4ma	-286mv	616mv	330mv	225mv
Assert	Negate	130	0mv	120nom	4.4ma	-286mv	528mv	242mv	137mv
Assert	Negate	130	0mv	110	4.4ma	-286mv	484mv	198mv	93mv
Assert	Negate	130	0mv	100	4.4ma	-286mv	440mv	154mv	49mv

Assert Negate 130 0mv 90 4.4ma -286mv 396mv 110mv 5mv

FAST-40 NOISE MARGIN CASES
Incident wave transitions

DRIVEN NEGATED --> ASSERTED:



V1 = (min terminator offset) + Imin * (max terminator resistance)/2

Vswing = Zline * Imin / 2

V2 = V1 - Vswing

Noise margin = V2 - (rcvr sensitivity + crosstalk) = | V2 - (-105mv) |

state1	state2	Rterm	Vterm	Zline	Idrvr	V1	Vswing	V2	Margin
Negate	Assert	130	130mv	160	4.4ma	416mv	-704mv	-288mv	183mv
Negate	Assert	130	130mv	140	4.4ma	416mv	-616mv	-200mv	95mv
Negate	Assert	130	130mv	120	4.4ma	416mv	-528mv	-112mv	7mv
Negate	Assert	130	130mv	110	4.4ma	416mv	-484mv	-68mv	-37mv

```
Negate      Assert      130   130mv 100   4.4ma        416mv      -440mv
       -24mv       -81mv

Negate      Assert      130   130mv  90   4.4ma        416mv      -396mv
        20mv      -125mv


Trying larger minimum drive currents:

Negate      Assert      130   130mv 100   5.0ma        425mv      -500mv
       -50mv       -55mv

Negate      Assert      130   130mv 100   6.0ma        490mv      -600mv
      -110mv         5mv

Negate      Assert      130   130mv 100   7.0ma        555mv      -700mv
      -145mv        40mv

Trying lower termination resistances (45-55 ohms):

Negate      Assert      110   130mv 100   5.0ma        375mv      -500mv
      -125mv        20mv
```

RECOMMENDATIONS

- Add a new state to be transitioned through when disconnecting from the bus. Connect a resistance between the positive and negative current sources. This resistance is in parallel with the transmission line, and will permit the SCSI device to exit from the LVDS bus without any assertion glitches.

- Consider lowering the termination resistance from 60 +/-5 ohms to 50 +/- 3 ohms.

- Specify tighter matching for differential mode resistors within a terminator chip.

- Raise drive current range from 4.4 - 6.0mA to 5.0 - 7.0ma

- Limit loaded line impedance to 100 ohms minimum.