SPI-2 LVDS Driver Tests

Communications Marketing
SPI-2 LVDS Driver Z
SPI-2 LVDS Waveform
SPI-2 LVDS Termination

Sourced from TERMPWR, Enabled Terminators only
Source 5 < 15 mA Open Circuit on power off
Sink < 200 uA (Noise Load) or Open Circuit for a Disabled Terminator

Ref 1.3V
1.3V +/- 0.1V

Diff Sense

20K

Low Frequency
Filter 50 - 60 Hz
0.1 uF

1.9 < 2.2V

High Power/EIA485 Differential

LV Diff

0.6 < 0.7V

Single Ended

High Impedance Receiver, even with power off

Ref 2.7V

Source/Sink

Ref 1.25V

4.7 uF

110

+75 mV 60°

Line -

150

-75 mV 60°

Line +

Closed for Single Ended

< 250 uA

* May Reflect the AC Impedance
Switches are up for Single Ended
Switches are down for Low Voltage Differential
SPI-2 LVDS Diff Sense

Differential Sense Bus

1.2 < 1.4 V Terminator
5 < 15 mA Source Current
< 200 uA Sink Current

+5V
+4.75V < 5.25V
1K
High Power/EIA485 Differential
Receiver threshold 0.8 to 2.0 V < 1 mA load
3.75V min with 1 mA for the receiver load
Diff Sense

1.2 < 1.4 V Terminator

Single Ended

Device & Termination Detection Circuit

Diff Sense
20K
1.9 < 2.2V

200K
0.1 uF
0.6 < 0.7V

High Power/EIA485 Differential
LV Diff
Single Ended

Communications Marketing
SPI-2 LVDS Bus

Diff Z = 115 < 160 Ohms
Single ended Z = 72 < 96 Ohms

1.25V

150 mV < 250 uA

Driver Current = 4.0 < 6.0 mA
Driver Current Delta between 0 and 1 < 0.5 mA

Receiver Threshold +/- 100 mV

Communications Marketing
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- Reviewed the document sections of SPI that will be effected by LVDF SPI.
- Studied the Diff Sense issues and set new values
- Reviewed common mode issues with each interface
- Reviewed the cost objectives of LVDS
- Defined the pinning for the based on Single ended, regenerated table done in Harrisburg, but not documented.
- Note: FAST-40 single ended would still be a longer distance than ATA. This should be a viable standard.
- FAST-40 and FAST-80 will require very low delta stub and capacitance for data, parity, ack and req signals. The additive effect of 7 or 15 devices will exceed the skew budget.
- Worked timing issues for FAST-40 and FAST-80, external drivers and receivers can not be used, there is no margin in the skew budget.
Agreements

- A single chip may work for both single ended (Async, 5, 10,20) or LVDS (FAST-40,80)
- No SE FAST-40
- No SE Signals in FAST-40
- Timing OK
- Diff sense is define with an autosense feature.
- low, (SE) all ground drivers shall be on.
- Pin outs OK
- Target of 15 pF maximum
- Current mode Driver, no Driver output impedance spec.
- Terminator bias with current limited, 100 mV at 250 microAmps maximum.
- No specified receiver hysteresis.
LVDS Power Calculations

- Transceiver power calculations for a 27 line device at 3.3 Volts + 10%.
- Maximum 21 Active Drivers on a 27 line device.
- 27 Active Receivers
- Driver control current 1 mA * 3.6 Volts, 3.6 mW * 21 Lines = 75.6 mW
- Driver power 4 mA * (3.6-.24) Volts, 13.6 mW * 21 Lines = 285.6 mW
- Receiver Power 2.5 mA * 3.6 Volts, 9 mW * 27 Lines = 243 mW
- Total Transceiver current 604.2 mW
LVDS - 6 mA Power

- Transceiver power calculations for a 27 line device at 3.3 Volts + 10%.
- Maximum 21 Active Drivers on a 27 line device.
- 6 Active Receivers
- Driver control current 1 mA * 3.6 Volts, 3.6 mW * 21 Lines = 75.6 mW
- Driver power 6 mA * (3.6-.36) Volts, 19.44 mW * 21 Lines = 408.24 mW
- Receiver Power 2.5 mA * 3.6 Volts, 9 mW * 6 Lines = 54 mW
- Total Transceiver current 537.84 mW