Accredited Standards Committee*
X3, Information Technology

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Reply to: Gene Milligan

To: Membership of X3T10

From: Larry Lamers, Secretary
Gene Milligan, Chair

Subject: Minutes of ATA Working Group - 9/19-22/95

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15. Adjournment

Results of Meeting

1. Opening Remarks

Gene Milligan, the ATA Working Group Chair, called the meeting to order at 9:00 a.m., Tuesday September 19, 1995. He thanked Quantum Corporation for hosting the meeting and Larry Lamers for taking the minutes.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated. It was announced that general information on X3T10 is available at the head table to any interested party.

2. Approval of Agenda

The draft agenda was approved.

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or organization directly and materially affected by X3T10's scope of work.

The following people attended the meeting:

name	company	telephone	email
Mr. Richard Kalish	Adaptec, Inc.	(408) 957-7169	rkalish@corp.adaptec.com
Mr. Tony Kwan	Adaptec, Inc.	(408) 945-8600	tkwan@corp.adaptec.com
Mr. Lawrence J. Lamers	Adaptec, Inc.	(408) 957-7817	ljlamers@aol.com
Mr. Dennis Pak	Apple Computer	(408) 974-4874	dennis.pak@apple.eworld.com
Mr. Ron Roberts	Apple Computer	(916) 677-5714	rkroberts@aol.com
Mr. Florey Lin	Cirrus Logic	(510) 226-2100 x3774	florey@cirrus.com
Mr. Joe Chen	Cirrus Logic Inc.	(510) 226-2101	chen@cirrus.com
Mr. Les Cline	Cirrus Logic Inc.	(510) 623-8300	lesc@corp.cirrus.com
Mr. Chi Wang	Cirrus Logic Inc.	(510) 249-4278	cwang@cirrus.com
Mr. Marc Noblitt	Conner Peripherals	(303) 682-8408	marc.noblitt@conner.com
Mr. Anthony Yang	Hitachi America Ltd.	(408) 653-0315	yang-a@halsp.hitachi.com
Mr. Dan Colegrove	IBM Corp.	(408) 256-1978	colegrove@vnet.ibm.com

Mr. Anthony E. Pione	IBM Corp.	(407) 443-1504	anthony_pione@bocaraton.ibm.com
Mr. Duncan Penman	IIX Consulting	(408) 730-2565	penman@netcom.com
Mr. LeRoy Leach	Maxtor Corp.	(303) 678-2828	leroy_leach@maxtor.com
Mr. Pete McLean	Maxtor Corp.	(303) 678-2149	pete_mclean@maxtor.com
Mr. Robin Freeze	Oak Technology, Inc.	(408) 737-0888 x644	robinf@oaktech.com
Mr. Curtis E. Stevens	Phoenix Technologies	(714) 440-8330	curtis_stevens@bannet.ptltd.com
Mr. Mark Evans	Quantum Corp.	(408) 894-4019	mevans@qntm.com
Mr. James McGrath	Quantum Corp.	(408) 894-4504	jmcgrath@qntm.com
Mr. Steve Reames	Reames Engineering	(719) 495-0141	reames@diskdrive.com
Mr. John Masiewicz	Seagate Technology	(408) 439-2152	
Mr. Gene Milligan	Seagate Technology	(405) 324-3070	gene_milligan@notes.seagate.com
Mr. John Wright	Seagate Technology	(408) 439-7431	johnw@cdg.seagate.com
Mr. Mike Yokoyama	Sony Electronics, Inc.	(408) 955-4344	masayuki@cppc.sel.sony.com
Mr. Patrick Mercer	SyQuest Technology Corp.	(510) 226-4215	patrick.mercer@syquest.com
Mr. Carl Bonke	Western Digital Corp.	(714) 932-7622	bonke@dt.wdc.com
Mr. Tom Hanan	Western Digital Corp.	(714) 932-7472	hanan_t@a1.wdc.com

4. Document Distribution

X3T10/2008D rev 4
X3T10/95-258 rev 3
X3T10/1120D rev 1

5. Review of Action Items

30) Larry Lamers to post a proposal that the 16-byte command packet should be defined as a transfer of a SCSI CDB as defined in an ANSI standard or X3T10 working draft. Carry over.
31) Curtis Stevens to prepare proposed flow charts for ATA-3. Completed.
32) Gene Milligan to follow-up with Compaq on the reported security patent. Completed.

6. ATA-2 - Project 0948 X3 [] (X3.279-199x, ATA-2)

The X3 letter ballot has not yet completed.

7. ATAPI - Project 1120D

7.1 ATAPI Working Draft Review [Hanan]

Tom Hanan suffered a back injury and was unable to provide the document for review as scheduled. The group discussed a number of items related to the difficulty in progressing the ATAPI document. Tom was able to provide an updated document on the day after it was scheduled and the group reviewed the update following the completion of the ATA-3 review.

Concern was expressed that the update was not complete in that the previously defined ATAPI IDENTIFY and SET FEATURES definitions have not been included in the document. The technical editor again agreed to include the missing items in the next draft.

7.2 Other ATAPI Items [] ()

Pete McLean noted that the ATAPI packet commands are not included in MMC. The MMC draft defines a SCSI command set for CD-ROM drives, including CD-Rs.

The group discussed various alternatives relative to the SFF 8020, MMC, 1120 ATAPI, and ATA.

Curtis Stevens moved and Pete McLean seconded that the objective to support configurations that have an ATA and an ATAPI device on the same cable be reaffirmed. The motion carried unanimously.

8. ATA-3 - Project 2008D

8.1 ATA-3 Working Draft Review [McLean]

Pete McLean distributed revision 4. The working group did a walk through of the changes and made further suggestions to be incorporated into the next revision.

Tom Hanan alluded to a possible patent issue with the normal output of 80h in 8.4 but declined to offer enough information for the committee to take any action. However Tom did request that a note be added to the CHECK POWER MODE that not all devices will return all values of the sector count register. This was agreed to by consensus.

Pete McLean moved that no entry in the command block registers indicates that the bit or register is not used by device and no entry in the error register indicates that the bit or register is not set by the device. The motion, as amended below, carried 11:0.

Jim McGrath moved and Rick Kalish seconded an amendment that the no entry bits or registers shall contain zero if they are written except for the device head register bit 7 and 5. The motion carried 8:3.

Joe Chen moved and Rick Kalish seconded that the HEAD register have bits 7 and 5 set to one and a note added that they are set to one for backward compatibility and may be reclaimed in a future standard. The motion carried 11:0.

8.2 DRQ & command block registers [] ()

Does DRQ active protect the command block registers at the end of a data transfer? Pete McLean will add the following wording to 6.2:.

> "Anytime a command is in progress, that is, from the time the Command register is written with the command until the device has completed the command and posted ending status, the device shall have either BSY or DRQ set to one. If the Command Block registers are read by the host when BSY or DRQ is set to one, the content of all register bits and fields except BSY and DRQ in the Status and Alternate Status registers is indeterminate. If the host writes to any Command Block register when BSY or DRQ is set to one, the results are indeterminate and may result in the command in progress ending with a command abort error. BSY and DRQ shall both be cleared to zero within 400 ns of INTRQ being asserted at the end of the last data transfer for a command."

8.3 t2i timing for MODE 0 Command Block Registers [] ()

What should the t2i timing be for MODE 0 Command Block Registers?. The group agreed that these entries should remain blank as they are in ATA-2.

8.4 Secure Mode features [] ()

Gene Milligan reported on a conversation with Ken Bush. Ken is following up to get a formal response on the letter concerning the security related patent.

Furthermore Ken stated that Compaq would like to see security capability retained in the ATA-3 standard. The group discussed the impact of the extended uncertainty over the inclusion of the security mode in the standard and the resultant extension of at least one de facto implementation along with the tradeoffs of multiple implementations.

Ron Roberts moved and Larry Lamers seconded that the Colegrove/IBM Secure Mode proposal be accepted as a replacement for the existing definition in ATA-3. The motion carried 10:0.

8.5 READ/WRITE LONG [] ()

The READ/WRITE LONG commands are currently optional. Should their implementation be made vendor specific? Tom Hanan moved and Curtis Stevens seconded that these commands remain optional in ATA-3 and not become vendor-specific The motion carried 9:1.

Jim McGrath moved and Rick Kalish seconded that a recommendation be included that READ LONG and WRITE LONG be used in indivisible pairs. Furthermore the committee will consider removing these commands in the next standard. The motion carried 10:0.

8.6 READ/WRITE MULTIPLE [] ()

Tom Hanan moved and Curtis Stevens seconded that the SET MULTIPLE command be mandatory. The motion carried 5:1.

Jim McGrath moved and Curtis Stevens seconded that while the command is mandatory for devices it is recommended that the host use the default value reported in the IDENTIFY DRIVE data and that the value used shall be 2, 4, 8, 16, 32, 64, or 128. The motion passed 6:0.

8.7 ATA Signal Integrity [Reames] ()

Steve Reames presented revision 1.02 of the Signal Integrity Annex. The group did a page by page review. The annex with the modifications recommended by the group will be included in the next revision of ATA-3.

8.8 ATA-3 Forwarding Letter Ballot Logistics [] ()

The ad hoc agreed that with the addition of the flow diagrams and the change in the security mode architecture, the anticipated letter ballot should be postponed until after the October meeting.

8.9 Strong Command Overlap and Command Queuing Proposal Update [McLean] (95-258)

Duncan Penman provided a series of questions and/or suggestions that were very helpful in a review of the proposal. He noted that an agreement on consistent terminology was essential for adequate documentation. He also pointed out that the state of the bus and the state of device need to be noted separately.

The group reviewed revision 3. The group requested state diagrams be added. There were mixed opinions on whether Release should always occur. For the purpose of the next revision Pete will assume that Release is conditional upon whether or not an “immediate” transfer is available.

Duncan also raised a question of when is the DMA engine initialized with tagged operations? This will need further discussion, the only obvious solution is waiting to setup the engine until after the SERVICE command has been issued but this may pose a serious performance penalty.

Should an interrupt be used at the end of PIO transfers to indicate end of command and provide status?
Should interrupts during read multiple operations be eliminated?
Should the READ PIO OVERLAP command be eliminated?
These questions will be addressed at the next meeting and feedback is solicited.

Jim McGrath moved and John Masiewicz seconded that READ PIO OVERLAP and WRITE PIO OVERLAP be removed. The motion was deferred to the next meeting to allow additional feedback.

What happens if the host sees a glitch handling proxy interrupt when changing from selecting device 0 to selecting device 1? Duncan Penman suggested a need to specify timings to prevent overlapped driving of INTRQ. Pete McLean suggested that changing to a positively asserted wire-or'd signal with a pull-down resistor and a pull-up transistor eliminates the need for proxy interrupts. The old and new devices could co-exist, however overlap

would only work with two new devices. John Masiewicz proposed that the host use the nIEN bit, which is the three-state control of the INTRQ signal, to prevent devices from simultaneously asserting INTRQ.

Curtis Stevens moved and Marc Noblitt seconded that further work on the ATA overlap proposal cease. The motion was deferred until the next meeting to allow additional feedback.

8.10 IDENTIFY DRIVE data in support of host requirements [] ()

Curtis Stevens stated that his proposal is not yet complete. There was some discussion on the topic. His proposal will be for a private data area on the drive using a READ SEGMENT and WRITE SEGMENT command to access it. This area would not be accessible to normal read/write operations.

8.11 Protocol Flow Charts [] ()

The flow charts as proposed will be incorporated into ATA-3. Participants are urged to review them in detail for the next meeting.

8.12 ANSI Editor's changes vis-à-vis ATA-3 [] ()

The consensus was to incorporate the ANSI editor's comments on ATA-2 into ATA-3.

8.13 New Changes to ATA-3 [] ()

8.13.1 SMART manufacturing date

Tom Hanan requested that a manufacturing date be added to the SMART data. He maintains that this will significantly reduce the volume of technical support phone calls.

Tom moved that the manufacturing date and an optional warranty field be added to the IDENTIFY DRIVE data. The motion failed due to lack of a second.

Curtis Stevens moved and Tom Hanan seconded that a manufacturing date and vendor specific field be added to the IDENTIFY DRIVE data. The motion failed 2:7.

Mark Evans reported that there is a request for other SMART information, power-on hours, power cycles and the number of CSS events.

8.13.2 SMART identify bits

The Chair reviewed a request he had received to add bits to indicate support for SMART and related the scenario that would require them. Upon further review the bits are not needed since the scenario does not conform to the SMART definition.

8.13.3 Removable bits

Tom Hanan reported a problem with controllers that set the removable bit but neither abort nor execute the removable commands which results in system lockups. Although the manufacturers of these controller cards should correct their non-compliant implementation Tom requested a statement be added to the standard as a patch to the problem.

Pete McLean moved and Rick Kalish seconded that this be considered in the next standard (ATA+PI and/or ATA-4). The discussion led to adding a note to LOCK and UNLOCK commands to warn those using these commands with devices that fake the reporting of removability. Accepted without objection. (Chairs note: the action taken makes the specific motion obsolete and should be considered as if it were a friendly and accepted amendment.)

8.13.4 Removable media modes 7.4.

Patrick Mercer distributed via Email his proposal for modifying the removable media bits. The consensus was to include this in the next revision.

9. Old Business

9.1 ATA+PI [McLean] (95-258r2)

Except for the discussion under item 8.9, there was no business to conduct. The new project proposal did not result in a recommendation by OMC but is going out for an X3 letter ballot.

9.2 New Technical Committee [] ()

.The recommendation for a New Technical committee did not result in a recommendation by OMC but is going out for an X3 letter ballot.

9.3 Open Issues List [] ()

9.3.1 clearing of pending interrupts and how it relates to writing the command register or reading the status register.

Action taken during the ATA-3 review apparently defused this issue and it will be deleted from the list.

9.3.2 when is DMA mode? see item g)

The device is in DMA mode whenever DMACK is asserted following its assertion of DMARQ whether it is selected or not. Until DMACK is asserted the device is in PIO mode.
The device exits DMA mode whenever DMACK is negated.
Rick Kalish volunteered to propose a DMA model.

9.3.3 concept of PIO transfers for register access (during DMA registers are not accessible) [data register > PIO; data port > DMA]

.It is assumed that the DMA model will also address this issue.

9.3.4 an annex is needed on the logical impact of shared cables. (Landis)

There has not been any proposals made and no discussion was offered.

9.4 ATA Mode X Analog Issues [] ()

The consensus was reaffirmed that further increases in data transfer will not be considered until the analog issues surrounding high transfer rates are resolved. After further testing, the mode 3 synchronous DMA proposal has been withdrawn until the analog issues have been resolved.

Investigation of improvements in the physical plant, drivers, receivers, cables, connectors, are being undertaken to add margin to the existing transfer modes as well as to form the basis for work on even higher transfer rates.

9.5 ATA Cable Issues and Definitions [McGrath] ()

WD tested 3.3 volts at various currents to determine the voltage drop. They ranged from negligible at 100 ma to 0.3 v at 1 amp. Some cross talk was noted in the DB 15 line (33.6 mV induced). The problems with inductance; pushing 100 ma or greater through 28 AWG wire; build-up of resistance in the connectors; all lead to agreement that routing power through conductor 20 is not a good idea.

Another method of providing 3 volt power for devices is needed.

Connector requirements:
fits in existing 4 contact connector slot
carries at least 4 different voltages with adequate ground
should be in volume production with at least 3 suppliers

A request will be made by Jim McGrath to add this to the SFF agenda for the Palm Springs, CA meeting.

10. New Business

10.1 Cables & Connectors[] ()

Pete McLean reported that the cable and connector folks at the last SFF meeting would undertake an investigation of the needs presented to them. A follow-up meeting is planned in Palm Springs, CA.

10.2 System Issues [Penman] ()

The list of candidates for consideration developed at the last meeting was:
Host Configuration Guidelines
IDE Bus Master Controller/PCI Interface
EDD > 8 GB BIOS OS
System Level Queuing and Overlap
Partition Sizes > 2 GB
System Level Error Recovery
.

10.3 Document Format and Distribution [Lamers] ()

Curtis Stevens moved and Pete McLean seconded that the working group and future technical committee adopt Word 6 as common format for distribution of documents and working drafts. The motion passed unanimously.

The consensus was that an electronic mailing is the preferred distribution method.

11. Call for Patents

Gene Milligan requested that anyone aware of any patents required for the proposals be disclosed early in accordance with the ANSI patent policy. He also pointed out that IBM has made a blanket offer of any of their patents that may be required by the interface standards.

As noted in earlier minutes the Secure Mode proposal involves patents pointed out by Pete McLean and he stated that a letter has been submitted by Maxtor. He also mentioned an IBM patent and Dan Colegrove noted that document 94-125 contains the letter regarding the ANSI patent policy.

Pete McLean reported that the change in Secure Mode made at this meeting will not impact Maxtor's response to the patent call.

12. Open Issues List

The list of open issues (using a running list designator) was reviewed as follows:
b) when is DMA mode? see item 9.3.2 & 9.3.3
Rick Kalish volunteered to develop a proposal.
c) need to add concept of PIO transfers for register access (during DMA registers are not accessible) [data register > PIO; data port > DMA] See item 9.3.3.
This needs a proposal - Jim McGrath volunteered.
e) an annex is needed on the logical impact of shared cables. (Landis)
Hale did not bring his proposal.

l) When is the DMA engine initialized with tagged operations?

13. Action Items

33) Pete McLean to prepare ATA-3 rev 5
34) Tom Hanan to prepare ATAPI rev 1
35) Pete McLean to prepare Overlap Proposal rev 4
36) Rick Kalish to prepare proposed DMA model
37) Jim McGrath to contact SFF regarding power connector

14. Future Meeting Schedule

The ad hoc meetings are authorized by the plenary for a maximum of two plenary meeting cycles. However meeting dates beyond that are blocked out for planning purposes to enable the dates should they be judged to be required by the plenary. In the event X3 authorizes the formation of a new technical committee no more than six per year of these blocked dates would be assigned for the plenary week. The group also discussed the need to minimize the number of meetings required to fit the needs of the industry.

October 17-19, 1995 at the Mariottt Hotel on Fashion Island in Newport Beach, CA hosted by Phoenix Technologies.
November 28-December 1, 1995 - at the WD facility in Irvine, CA hosted by Western Digital.
Proposed dates for 1996 are:
January 23-26, 1996
February 20-23, 1996
March 26-29, 1996
April 23-26, 1996
May 21-24, 1996
June 18-21, 1996
July 30-August 2, 1996
August 20-23, 1996
September 24-27, 1996
October 22-25, 1996
November 12-15, 1996
December 1996 - No Meeting

The starting time for the meetings is 9:00 am.

The ad hoc agreed to revert back to the recommendation of the Longmont meeting and not have a meeting week map since its use had resulted in a half day or more of lost time at this meeting. The meeting adjourned Friday after completion of all agenda items.