Accredited Standards Committee*
X3, Information Technology

Doc. No.: X3T10/95-328r0
Date: 04/18/98
Project:
Ref. Doc.:
Reply to: Gene Milligan

To: Membership of X3T10

From: Larry Lamers, Secretary
Gene Milligan, Chair

Subject: Minutes of ATA Working Group - 9/19-22/95

Agenda

1. Opening Remarks
2. Approval of Agenda
3. Attendance and Membership
4. Document Distribution
5. Review of Action Items
6. ATA-2 - Project 0948
    6.1 X3 Public Review Comments [] ()
7. ATAPI - Project 1120D
    7.1 ATAPI Working Draft Review [Hanan]
    7.2 Other ATAPI Items [] ()
8. ATA-3 - Project 2008D
    8.1 ATA-3 Working Draft Review [McLean]
    8.2 DRQ & command block registers [] ()
    8.3 t2i timing for MODE 0 Command Block Registers [] ()
    8.4 Strong Command Overlap and Command Queuing Proposal Update [] ()
    8.5 IDENTIFY DRIVE data in support of host requirements [Steven's] ()
    8.6 Secure Mode features [] ()
    8.7 READ/WRITE LONG [] ()
    8.8 READ/WRITE MULTIPLE [] ()
    8.9 ATA Signal Integrity [] ()
    8.10 ATA-3 Forwarding Letter Ballot Logistics [] ()
    8.11 Strong Command Overlap and Command Queuing Proposal Update [] ()
    8.12 IDENTIFY DRIVE data in support of host requirements [] ()
    8.13 Protocol Flow Charts [] ()
    8.14 ANSI Editor's changes vis-à-vis ATA-3 [] ()
    8.15 New Changes to ATA-3 [] ()
        8.15.1 SMART manufacturing date
        8.15.2 SMART identify bits
        8.15.3 Removable bits
        8.15.4 Removable media modes 7.4.
9. Old Business
    9.1 ATA+PI [McLean] (95-258r2)
    9.2 New Technical Committee [] ()
    9.3 Open Issues List [] ()
        9.3.1 clearing of pending interrupts and how it relates to writing the command register or reading the status register.

9.3.2 when is DMA mode? see item g)
9.3.3 concept of PIO transfers for register access (during DMA registers are not accessible) [data register > PIO; data port > DMA]
9.3.4 an annex is needed on the logical impact of shared cables. (Landis)
9.4 ATA Mode X Analog Issues [Hanan] ()
9.5 ATA Cable Issues and Definitions [McGrath] ()

10. New Business
10.1 Cables & Connectors[] ()
10.2 System Issues [Penman] ()
10.3 Document Format and Distribution [Lamers] ()

11. Call for Patents

12. Open Issues List

q13. Action Items

14. Future Meeting Schedule

15. Adjournment

Results of Meeting

1. Opening Remarks

Gene Milligan, the ATA Working Group Chair, called the meeting to order at 9:00 a.m., Tuesday September 19, 1995. He thanked Quantum Corporation for hosting the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated. It was announced that general information on X3T10 is available at the head table to any interested party.

2. Approval of Agenda

The draft agenda was approved.

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or organization directly and materially affected by X3T10's scope of work.

The following people attended the meeting:

name	company	telephone	email
Mr. Richard Kalish	Adaptec, Inc.	(408) 957-7169	rkalish@corp.adaptec.com
Mr. Tony Kwan	Adaptec, Inc.	(408) 945-8600	tkwan@corp.adaptec.com
Mr. Lawrence J. Lamers	Adaptec, Inc.	(408) 957-7817	ljlamers@aol.com
Mr. Dennis Pak	Apple Computer	(408) 974-4874	dennis.pak@apple.eworld.com
Mr. Ron Roberts	Apple Computer	(916) 677-5714	rkroberts@aol.com
Mr. Florey Lin	Cirrus Logic	(510) 226-2100 x3774	florey@cirrus.com
Mr. Joe Chen	Cirrus Logic Inc.	(510) 226-2101	chen@cirrus.com
Mr. Les Cline	Cirrus Logic Inc.	(510) 623-8300	lesc@corp.cirrus.com
Mr. Chi Wang	Cirrus Logic Inc.	(510) 249-4278	cwang@cirrus.com
Mr. Marc Noblitt	Conner Peripherals	(303) 682-8408	marc.noblitt@conner.com
Mr. Anthony Yang	Hitachi America Ltd	(408) 653-0315	yang-a@halsp.hitachi.com
Mr. Dan Colegrove	IBM Corp.	(408) 256-1978	colegrove@vnet.ibm.com

Mr Anthony E. Pione	IBM Corp.	(407) 443-1504	anthony_pione@bocaraton.ibm.com
Mr. Duncan Penman	IIX Consulting	(408) 730-2565	penman@netcom.com
Mr. LeRoy Leach	Maxtor Corp.	(303) 678-2828	leroy_leach@maxtor.com
Mr. Pete McLean	Maxtor Corp.	(303) 678-2149	pete_mclean@maxtor.com
Mr. Robin Freeze	Oak Technology, Inc	(408) 737-0888 x644	robinf@oaktech.com
Mr. Curtis E. Stevens	Phoenix Technologies	(714) 440-8330	curtis_stevens@bannet.ptltd.com
Mr. Mark Evans	Quantum Corp.	(408) 894-4019	mevans@qntm.com
Mr. James McGrath	Quantum Corp.	(408) 894-4504	jmcgrath@qntm.com
Mr. Steve Reames	Reames Engineering	(719) 495-0141	reames@diskdrive.com
Mr. John Masiewicz	Seagate Technology	(408) 439-2152	
Mr. Gene Milligan	Seagate Technology	(405) 324-3070	gene_milligan@notes.seagate.com
Mr. John Wright	Seagate Technology	(408) 439-7431	johnw@cdg.seagate.com
Mr. Mike Yokoyama	Sony Electronics, Inc.	(408) 955-4344	masayuki@cppc.sel.sony.com
Mr. Patrick Mercer	SyQuest Technology Corp.	(510) 226-4215	patrick.mercer@syquest.com
Mr. Carl Bonke	Western Digital Corp.	(714) 932-7622	bonke@dt.wdc.com
Mr. Tom Hanan	Western Digital Corp.	(714) 932-7472	hanan_t@a1.wdc.com

4. Document Distribution

X3T10/2008D rev 4

5. Review of Action Items

30) Larry Lamers to post a proposal that the 16-byte command packet should be defined as a transfer of a SCSI CDB as defined in an ANSI standard or X3T10 working draft. Carry over.
31) Curtis Stevens to prepare proposed flow charts for ATA-3. Completed.
32) Gene Milligan to follow-up with Compaq on the reported security patent. Carry over.

6. ATA-2 - Project 0948

6.1 X3 Public Review Comments [] ()

X3.279-199x, ATA-2,

7. ATAPI - Project 1120D

7.1 ATAPI Working Draft Review [Hanan]

Tom Hanan did not show up due to a medical problem.

7.2 Other ATAPI Items [] ()

Pete McClean noted that the ATAPI packet commands are not included in MMC. The MMC draft defines an SCSI command set for CD-ROM drives, including CD-Rs.

Discussion on the current SFF tack regarding 8020; MMC; and ATA.

Curtis Stevens moved and Pete McLean seconded that the objective to support configurations that have an ATA and an ATAPI device on the same cable be reaffirmed. The motion carried unanimously.

8. ATA-3 - Project 2008D

8.1 ATA-3 Working Draft Review [McLean]

Pete McLean distributed revision 4. The working group did a walkthrough of the changes and made further suggestions to be incorporated into the next revision.

Possible patent issue with the normal output of 80h in 8.4.

Tom Hanan requested that a note be added to the CHECK POWER MODE that not all devices will return all values of the sector count register. Agreed by consensus.

Pete McLean moved that no entry in the command block registers indicates that the bit or register is not used by device and no entry in error register indicates that the bit or register is not set by the device. The motion carried 11:0.

Jim McGrath moved and Rick Kalish seconded an amendment that the no entry bits or registers shall contain zero if they are written except for the device head register bit 7 and 5. The motion carried 8:3.

Joe Chen moved and Rick Kalish seconded that the HEAD register have bits 7 and 5 set to one and a note added that they are set to one for backward compatibility and may be reclaimed in a future standard. The motion carried 11:0.

8.2 DRQ & command block registers [] ()

Does DRQ active protect the command block registers at the end of a data transfer? Pete McLean will add the following wording to 6.2:.

> Anytime a command is in progress, that is, from the time the Command register is written with the command until the device has completed the command and posted ending status, the device shall have either BSY or DRQ set to one. If the Command Block registers are read by the host when BSY or DRQ is set to one, the content of all register bits and fields except BSY and DRQ in the Status and Alternate Status registers is indeterminate. If the host writes to any Command Block register when BSY or DRQ is set to one, the results are indeterminate and may result in the command in progress ending with a command abort error. BSY and DRQ shall both be cleared to zero within 400 ns of INTRQ being asserted at the end of the last data transfer for a command.

8.3 t2i timing for MODE 0 Command Block Registers [] ()

What should the t2i timing be for MODE 0 Command Block Registers?. No input - no action taken.

8.4 Secure Mode features [] ()

Gene Milligan reported on a conversation with Ken Bush. Ken was following up with his management to get a formal response.

Furthermore Ken stated that Compaq is considering implementing a secure mode feature in future computer systems and would like to see it remain in the ATA-3 working draft.

Ron Roberts moved and Larry Lamers seconded that the Colegrove/IBM Secure Mode proposal be accepted as a replacement for the existing definition in ATA-3. The motion carried 10:0.

8.5 READ/WRITE LONG [] ()

The READ/WRITE LONG commands are currently optional. Should their implementation be made vendor specific? Tom Hanan moved and Curtis Stevens seconded that these commands remain optional in ATA-3 and not become vendor-specific The motion carries 9:1.

Jim McGrath moved and Rick Kalish seconded that a recommendation be included that READ LONG and WRITE LONG be used in indivisible pairs. Furthermore the committee will consider removing these commands in the next standard. The motion carried 10:0.

8.6 READ/WRITE MULTIPLE [] ()

Tom Hanan moved and Curtis Stevens seconded that SET MULTIPLE command be mandatory. The motion carries 5:1.

Jim McGrath moved and Curtis Stevens seconded that while it is mandatory for devices it is recommended that the host use the default value reported in the IDENTIFY DRIVE data; this value shall be 2, 4, 8, 16, 32, 64, or 128. The motion passed 6:0.

8.7 ATA Signal Integrity [Reames] ()

Steve Reames presented revision 1.02 of the Signal Integrity Annex. The group did a page by page review. The annex with the comments generated will be included in the next revision of ATA-3.

8.8 ATA-3 Forwarding Letter Ballot Logistics [] ()

.

8.9 Strong Command Overlap and Command Queuing Proposal Update [McLean] (95-258)

The group reviewed revision 3. The group requested state diagrams be added. Pete will assume that Release happens.

Duncan Penman questioned whether or not release was needed. He also pointed out that the state of the bus and the state of device need to be noted separately.
Duncan also raised a question of when is the DMA engine initialized with tagged operations? This will need further discussion, the only obvious solution, waiting to setup the engine until after the SERVICE command has been issued poses a serious performance penalty.

Should an interrupt at the end of PIO transfers to indicate end of command and provide status?.
Should interrupts during read multiple operations be eliminated?
Should the READ PIO OVERLAP command be eliminated?
These questions will be decided at the next meeting.

Jim McGrath moved and John Masiewicz seconded that READ PIO OVERLAP and WRITE PIO OVERLAP be removed. The motion is deferred to next meeting.

What happens if the host sees a glitch handling proxy interrupt when changing from selecting device 0 to selecting device 1?

Duncan Penman suggested a need to specify timings to prevent overlapped driving of INTRQ. This potentially has interpretability.

Pete McLean suggested that changing to a positively asserted wire-or'd signal with a pull-down resistor and a pull-up transistor eliminates the need for proxy interrupts. The old and new devices could co-exist, however overlap would only work with two new devices. This idea needs some further exploration.

John Masiewicz offered an alternative. He proposed that the host use the nIEN bit, which is the tristate control on INTRQ signal, to prevent devices from simultaneously asserting INTRQ.

Curtis Stevens moved and Marc Nobliltt seconded that further work on the ATA overlap proposal cease. Deferred until the next meeting.

8.10 IDENTIFY DRIVE data in support of host requirements [] ()

Curtis Stevens stated that his proposal is not yet complete. There was some discussion on the topic. His proposal will be for a private area on the drive using a READ SEGMENT and WRITE SEGMENT command to access it. This area would not be accessible to normal read/write operations.

8.11 Protocol Flow Charts [] ()

The flow charts as proposed will be incorporated into ATA-3.

8.12 ANSI Editor's changes vis-à-vis ATA-3 [] ()

The consensus was to incorporate the ANSI editor's comments on ATA-2 into ATA-3.

8.13 New Changes to ATA-3 [] ()

8.13.1 SMART manufacturing date

Tom requested that a manufacturing date be added to the SMART data. He maintains that this will significantly reduce the volume of technical support phone calls.

Tom moved that the manufacturing date and optional warranty be added to the IDENTIFY DRIVE data. The motion failed due to lack of a second.

Curtis Stevens moved and Tom Hanan seconded that a manufacturing date and vendor specific field be added to the IDENTIFY DRIVE data. The motion failed 7:2.

Mark Evans reported that there is a request for other SMART information, power-on hours, power cycles and css.

8.13.2 SMART identify bits

Upon further review these are not needed.

8.13.3 Removable bits

A problem has been identified with controllers that set the removable bit that results in system lockups This problem is for the controller cards to correct their implementation.

Pete McLean moved and Rick Kalish seconded that this be considered in the next standard. Deferred.

Add a note to LOCK and UNLOCK commands to warn of using these commands with devices that fake the reporting of removability. Accepted.

8.13.4 Removable media modes 7.4.

Patrick Mercer distributed via Email his proposal for modifying the removable media bits. The consensus was to include this in the next revision.

9. Old Business

9.1 ATA+PI [McLean] (95-258r2)

.

9.2 New Technical Committee [] ()

.

9.3 Open Issues List [] ()

9.3.1 clearing of pending interrupts and how it relates to writing the command register or reading the status register.

No action needed. Item will be deleted from list.

9.3.2 when is DMA mode? see item g)

The device is in DMA mode whenever DMACK is asserted following its assertion of DMARQ whether it is selected or not. Until DMACK is asserted the device is in PIO mode.
The device exits DMA mode whenever DMACK is negated.
Rick Kalish volunteered to document these state changes.

9.3.3 concept of PIO transfers for register access (during DMA registers are not accessible) [data register > PIO; data port > DMA]

.

9.3.4 an annex is needed on the logical impact of shared cables. (Landis)

No action taken.

9.4 ATA Mode X Analog Issues [] ()

The consensus was that futher increases in data transfer will not be considered until the analog issues surrounding PIO mode 4 and DMA mode 2 are resolved.

Investigation of improvements in the physical plant, drivers, recievers, cables, connectors, are being undertaken to increase the reliability of existing transfer modes.

GENE - YOU NEED TO MAKE THIS POLITICALLY ACCEPTABLE.

After further testing, the mode 3 synchronous DMA proposal has been withdrawn until the above goals have been met.

9.5 ATA Cable Issues and Definitions [McGrath] ()

WD tested 3.3 volts at various currents to determine the voltage drop. They ranged from negligible at 100 ma to 0.3 v at 1 amp. Some cross talk was noted in the DB 15 line (33.6 mv induced). The problems with inductance; pushing 100 ma or greater through 28 AWG wire; build-up of resistance in the connectors; all lead to agreement that routing power through conductor 20 is not a good idea.

Another method of providing 3 volt power for devices is needed.

Connector requirements:
- fits in existing 4 contact connector slot
- carries at least 4 different voltages with adequate ground
- should be in volume production with at least 3 suppliers

A request will be made bt Jim McGrath to add this to the SFF agenda for the Palm Springs, CA meeting.

10. New Business

10.1 Cables & Connectors[] ()

Pete McLean reported that the cable and connector folks at the last SFF meeting would undertake an investigation of the needs presented to them. A followup meeting is planned in Palm Springs, CA.

10.2 System Issues [Penman] ()

The list of candidates for consideration developed at the last meeting was:

Host Configuration Guidelines
IDE Bus Master Controller/PCI Interface
EDD > 8 GB BIOS OS
System Level Queuing and Overlap
Partition Sizes > 2 GB
System Level Error Recovery

.

10.3 Document Format and Distribution [Lamers] ()

Curtis Stevens moved and Pete McLean seconded that the working group and future technical committee adopt Word 6 as common format for distribution of documents and working drafts. The motion passed unanimously.

The consensus was that an electronic mailing is the preferred distribution method.

11. Call for Patents

Gene Milligan requested that anyone aware of any patents required for the proposals be disclosed early in accordance with the ANSI patent policy. He also pointed out that IBM has made a blanket offer of any of their patents that may be required by the interface standards.

As noted in earlier minutes the Secure Mode proposal involves patents pointed out by Pete McLean and he stated that a letter has been submitted by Maxtor. He also mentioned an IBM patent and Dan Colegrove noted that document 94-125 contains the letter regarding the ANSI patent policy. Gene observed that he has not heard as yet what Compaq's response was to the patent letter from the X3T10 Chair John Lohmeyer.

12. Open Issues List

The list of open issues was reviewed as follows:

a) clearing of pending interrupts and how it relates to writing the command register or reading the status register. The

b) when is DMA mode? see item

Rick Kalish volunteered to develop a proposal.

c) need to add concept of PIO transfers for register access (during DMA registers are not accessible) [data register > PIO; data port > DMA]

This needs a proposal - Jim McGrath volunteered.

e) an annex is needed on the logical impact of shared cables. (Landis)

Hale did not bring his proposal.

l) When is the DMA engine initialized with tagged operations?

13. Action Items

33) Pete McLean to prepare ATA-3 rev 5
34) Tom Hanan to prepare ATAPI rev 1
35) Pete McLean to prepare Overlap Proposal rev 4
36) Rick Kalish to prepare When is DMA proposal

37) Jim McGrath to contact SFF regarding power connector
38) Curtis Stevens to prepare OS private area proposal

14. Future Meeting Schedule

The ad hoc meetings are authorized by the plenary for a maximum of tow plenary meeting cycles. However meeting dates beyond that are blocked out for planning purposes to enable the dates should they be judged to be required by the plenary. In the event X3 authorizes the formation of a new technical committee no more than six per year of these blocked dates would be assigned for the plenary week. The group also discussed the need to minimize the number of meetings required to fit the needs of the industry.

September 19-22, 1995 at the Red Lion in San Jose, CA hosted by Quantum.
October 17-20, 1995 at the Mariottt Hotel on Fashion Island in Newport Beach, CA hosted by Phoenix Technologies.
November 28-December 1, 1995 - at the WD facility in Irvine, CA hosted by Western Digital.
Proposed dates for 1996 are:
January 23-26, 1996
February 20-23, 1996
March 26-29, 1996
April 23-26, 1996
May 21-24, 1996
June 18-21, 1996
July 30-August 2, 1996
August 20-23, 1996
September 24-27, 1996
October 22-25, 1996
November 12-15, 1996
December 1996 - No Meeting

The starting time for the meetings is 9:00 am.

The meeting week agreed to by the ad hoc for the September meeting is:

	Tuesday	Wednesday	Thursday	Friday
9:00 am - 12:30 p.m.	ATAPI	ATA-3	ATA-3	ATA Futures
2:00 p.m. - 5:30 p.m.	ATAPI	ATA-3	ATA-3	ATA Futures

Note: The attendees may elect to have working lunch sessions on any of these days.

ATA Futures -
- cable annex (2 hours)
- overlap & queuing (2 hours)
- new projects (1 hour)
- other issues (2 hours)
- analog issues (2 hours)
- connector issues (brief report ~ 0 hours)

ATA-3
- ATA-3 issues
- document review

ATAPI
- ATAPI issues
- document review

15. Adjournment

The meeting adjourned Friday at 2:30 p.m.