Accredited Standards Committee*
X3, Information Technology

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Date: August 28, 1995
Project:
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Reply to: Gene Milligan

To: Membership of X3T10

From: Larry Lamers, Secretary
Gene Milligan, Chair

Subject: Minutes of ATA Working Group Meeting
San Jose, CA --August 22-25, 1995

Agenda

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   7.3 Strong Command Overlap and Command Queuing Proposal Update
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10. New Business
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11. Call for Patents

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Results of Meeting

1. Opening Remarks

Gene Milligan, the ATA Working Group Chair, called the meeting to order at 9:00 a.m., Tuesday August 22, 1995. He thanked Quantum Corporation for hosting the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated. It was announced that general information on X3T10 is available at the head table to any interested party.

2. Approval of Agenda

The draft agenda was approved.

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or organization directly and materially affected by X3T10's scope of work.

The following people attended the meeting:

name	company	telephone	email
Mr. Richard Kalish	Adaptec, Inc.	(408) 957-7169	rkalish@corp.adaptec.com
Mr. Tony Kwan	Adaptec, Inc.	(408) 945-8600	tkwan@corp.adaptec.com
Mr. Lawrence J. Lamers	Adaptec, Inc.	(408) 957-7817	ljlamers@aol.com
Mr. Kevin James	Advanced Micro Devices	(408) 749-7523	kevin.james@amd.com
Mr. Charles Brill	AMP, Inc.		cebrill@amp.com
Mr. Ron Roberts	Apple Computer	(916) 677-5714	rkroberts@aol.com
Mr. Richard Schnell	Apple Computer	(408) 974-5411	schnell2@eworld.com
Mr. Joe Chen	Cirrus Logic Inc.	(510) 226-2101	chen@cirrus.com
Mr. Les Cline	Cirrus Logic Inc.	(510) 623-8300	lesc@corp.cirrus.com
Mr. Marc Noblitt	Conner Peripherals	(303) 682-8408	marc.noblitt@conner.com
Mr. Hale Landis	Consultant	(303) 548-0567	landis@sugs.tware.com
Mr. Tim Norman	FMI (Fujitsu)	(408) 922-8928	tim.norman@fmi.fujitsu.com
Mr. Keji Watanabe	FMI (Fujitsu)	(408) 922-9066	
Mr. Anthony Yang	Hitachi America Ltd	(408) 653-0315	
Mr. Dan Colegrove	IBM Corp.	(408) 256-1978	colegrove@vnet.ibm.com
Mr. Duncan Penman	IIX Consulting	(408) 730-2565	penman@netcom.com
Mr. LeRoy Leach	Maxtor Corp.	(303) 678-2828	leroy_leach@maxtor.com
Mr. Pete McLean	Maxtor Corp.	(303) 678-2149	pete_mclean@maxtor.com
Mr. Jerry Kachlic	Molex		
Mr. Wayne Baldwin	Oak Technology	(408) 737-0888	wayneb@oaktech.com
Mr. Robin Freeze	Oak Technology	(408) 737-0888	robinf@oaktech.com
Mr. Jesse Kup	Oak Technology, Inc.	(408) 737-0888	jessek@oaktech.com
Mr. Chung-De Li	Oak Technology, Inc.	(408) 737-0888	
Mr. Min-Yi Li	Oak Technology, Inc.	(408) 737-0888	
Ms. Kristine Nguyen	Oak Technology, Inc.	(408) 737-0888	
Mr. Daniel Wu	Panasonic Industrial Co.	(4080 262-2200	

Mr. Curtis E. Stevens	Phoenix Technologies	(714) 440-8330	curtis_stevens@bannet.ptltd.com
Mr. Kelvin Kao	Promise Technology, Inc.	(408) 452-0948	kelvin-kao@promise.com
Mr. Mark Evans	Quantum Corp.	(408) 894-4019	mevans@qntm.com
Mr. Farbod Falakfarsa	Quantum Corp.	(408) 894-4066	ffalakfa@qntm.com
Mr. James McGrath	Quantum Corp.	(408) 894-4504	jmcgrath@qntm.com
Mr. Gene Milligan	Seagate Technology	(405) 324-3070	gene_milligan@notes.seagate.com
Mr. Ron Werbow	Seagate Technology	(805) 582-3815	ron_werbow@notes.seagate.com
Mr. Patrick Mercer	SyQuest Technology Corp.	(510) 226-4000	patrick.mercer@syquest.com
Mr. Brett Philip	TempFlex, Inc.	(408) 739-1236	
Mr. Yas Hashimoto	Toshiba America Info. Sys.	(408) 451-6960	
Mr. Tokuyuki Totani	Toshiba America Info. Sys.	(408) 451-6960	
Mr. Prakash Kamath	Weitek Corp.	(408) 522-7562	prakash@agni.weitek.com
Mr. Tom Hanan	Western Digital Corp.	(714) 932-7472	hanan_t@a1.wdc.com
Mr. Devon Worrell	Western Digital Corp.	(714) 932-7042	worrell@dt.wdc.com

4. Document Distribution

X3T10/1120D revision 0.3
X3T10/95-306r1 - Proposal to Modify the SECURE MODE feature set

5. Review of Action Items

28) Pete McLean to check with PCMCIA on removal of 8-bit transfers. Completed.
29) Jim McGrath to supply copyright release for annex F document. Completed.

6. ATA-2 - Project 0948

6.1 X3 Public Review Comments (If Any) - Finch]

X3.279-199x, ATA-2, completed its public review on August 8, 1995 without comments. The pre-edit by ANSI is expected to be completed by the end of August.

7. ATA-3 - Project 2008D

7.1 ATA-3 Working Draft Review [McLean]

Pete McLean reported that PCMCIA did not have any objection to the removal of the 8-bit data transfer mode controlled by the Set Features command. However 8-bit data transfer mode would continue to be a requirement for PC cards as controlled by the PC protocol and not by Set Features.

Curtis Stevens moved and Larry Lamers seconded that 8-bit data transfer mode be removed from ATA-3. The motion carried 10:0.

What happens to IOCS16? The current spec would leave IOCS16 pulled high. This could be a compatibility issue with old systems. Not of concern to the group.

During the review of the S.M.A.R.T. sections there was an objection expressed to a single opcode that both transfers data and does not transfer data depending upon specific control bits. The group recommended that rather than changing the definition in ATA-3 a warning be included addressing this behavior.

The group agreed that if S.M.A.R.T. is supported in the device, SMART DISABLE OPERATIONS, SMART ENABLE OPERATIONS, and SMART RETURN STATUS are mandatory. The other S.M.A.R.T. commands are optional.

Curtis Stevens moved and Ron Roberts seconded that the may be changed to shall for effect of soft reset on default parameters. The motion failed 1:6.

Curtis Stevens moved and Tom Hanan seconded that SET FEATURES be mandatory. The motion carried unanimously.

7.2 ATA signal integrity Annex

Steve Reames reviewed changes to Annex Q through page 14. He promised to complete the changes and provide the file for incorporation into the next revision of ATA-3.

7.3 Strong Command Overlap and Command Queuing Proposal Update

Marc Noblitt presented a list of questions on ATA overlap which resulted in the following:

item 1 - delete two sentences containing 50 us in 7.*.1.3
item 2 - change to ending status is abort
item 3 - specific registers added: tag, status, byte count, error,
item 4 - add an '..if idle..'' and the may changed to shall in 7.*.1.6
item 5 - clarify the working, add table to clarify register usage, move word 49 to 73 & low order bits are queue depth, time in microseconds typical,
item 6 - text is the additional text
item 7 - add definitions from ATAPI.
item 8 - see item 5.
item 9 - not changed
item 10 - yes, most likely
item 11 - everyone invited to prepare and present their favorite method.

Also clarify the clearing of the pending interrupt.

7.4 IDENTIFY DRIVE data in support of host requirements [Stevens]

Curtis will put a proposal on the reflector.

7.5 AC Characteristics [Reames] ()

Steve Reames presented material that indicates that the 100 pF test capacitive load in Table 4 is incorrect. Due to the propagation delays the actual load seen by the driver is significantly less because the loads are distributed along the bus and not all seen at once.

The consensus was to change to 40 pF test capacitive load in Note of Table 4 (X3T10/2008 rev3).

Tom Hanan moved and Jim McGrath seconded that the capacitance of devices (not hosts) be changed to 20 pF maximum. The motion carried 10:0.

Steve also want to change the 10%-90% to a slew rate specification. There was objection to making such a change at this stage in ATA-3 but consensus to discuss slew rates in the signal annex.

7.6 Proposal to modify SECURE MODE feature set [Totani] (95-306r1)

Mr. Totani presented a proposal to modify the SECURE MODE feature set in ATA-3. The discussion of the proposed modifications opened up a general discussion of security approaches. There was a lengthy discussion that did not reach consensus.

Curtis Stevens moved and Ron Werbow seconded that a vote on removal of SECURE MODE be taken at the next meeting pending input from interested parties. The motion carried 9:4.

Pete McLean indicated that he voted no because he believes that security will be required and having a uniform implementation is worthwhile and that the proposed modifications have merit in furthering this aim.

The attendees agreed to contact system manufacturers to seek their input on the SECURE MODE features set.

8. ATAPI - Project 1120D

8.1 ATAPI Working Draft Review [Hanan]

Tom Hanan reviewed the revision 0.3 document. Tom noted that the ATAPI IDENTIFY DRIVE command did not get incorporated due to work on other documents, and the conversion of the graphics into a format that allows for a more portable document is yet to be completed. Also, the illustration in the scope clause has not been modified to incorporate the agreed to changes.

Larry Lamers noted that the 16-byte command packet should be defined as a transfer of a SCSI CDB as defined in an ANSI standard or X3T10 working draft. Larry also noted that other interfaces utilizing the ATAPI protocol may need larger packet sizes (e.g. 64-bytes). These topics should also be discussed further by MMC.

Tom agreed to rewrite parts of clause 3 to deal with the limitations of the ATAPI protocol specifically instead of by reference to SCSI commands. Also references to the contents of the packet will change to indicate that these will be defined in profiles or other standards.

Tom Hanan intends to solicit comments on dealing with the architectural issue of the contents of ATAPI packets modifying the behavior of the protocol layer.

8.2 Other ATAPI Items [] ()

None.

9. Old Business

9.1 ATA+PI [McLean] (95-258r2)

Due to the lead time from X3T10 paper plus electronic copies to the project proposal and supporting documents to X3 paperless distribution, OMC did not address this topic and have scheduled the item for their October meeting.

9.2 New Technical Committee [] ()

Same as 9.1 discussion.

9.3 ATA Mode X Analog Issues [Hanan] ()

Driver Technologies -
low voltage (LV) single-ended other than TTL compatible, not necessarily compatible with existing drivers.
low voltage differential (LVD) - differential (8-bit data path) based on SCSI Fast-40 technology.

Using LV the resonance imparted to the cable is reduced, however the noise immunity is lowered.
Jim McGrath stated that parallel termination is another way to achieve MODE 3 DMA with existing driver technology. Tom believes that using LV allows 33 MB/sec with today's cable. Using LVD in the ATX (6-inch cable) 45 MB/sec should be achievable. Further work is needed.

10. New Business

10.1 Cables & Connectors[] ()

Tom Hanan wants to determine the maximum transfer speed with existing cables and switching levels. The next degree of freedom may be to allow changes in the switching levels. After that the proposed next step is to use the 16 data signals as an 8-bit differential path. However this step would require double the transfer rate just to maintain the existing data rate.

Brett Philip of TempFlex noted that a cable using PTFE dielectric can significantly reduce the crosstalk. This cable is currently being used in some high-transfer rate SCSI systems. Brett agreed to provide an indication of the inherent cost factors of the high dielectric cable compared to today's ATA cables to assess their long term viability in the ATA application.

Jim McGrath proposes using cable select to enable termination on the end device. However this requires a singular implementation of cable select. Pete McLean stated the simplest solution is to have a single drive installation be device one only. Jim objected on the basis that the device one only configuration would require the BIOS to tell the drives how many drives so the drives could configure. Jim agreed to provide a proposal based upon cable select.

Tom Hanan stated that 3 volt devices are coming. He suggested using the key pin (pin 20) to provide 3 volts to the drive. On 6-inch cables he expects a 200 mv drop. This translates into drive electronics operating on 2.5 v D.C. minimum. There is a specification being developed by Intel, ATX, that specifies the location of drives within an enclosure that would allow for shorter (e.g., 6-inch) cables.

Jim McGrath asked for ideas on modifications to the connector that could help. Brett noted that adding grounds would reduce the impedance. Pete McLean observed that there is significant ground bounce due to sourcing sixteen signals with only four return paths.

Topics agreed to for further discussion were: Cable, Termination (CSEL), ATX 6-inch, ATX 3 volt.

The proposed answer for termination enable is to ignore the harmful effects of a six-inch (or for new structures less) stub and let the drives enable their terminators if they determine they should. This means that ATA-3 needs to change and recommend the master be placed on the connector closest to the host. Can the termination be incorporated into the silicon?

Jim requested a footnote in ATA-3 that switchable terminators are being considered for future standards and master drives need to be able to determine whether or not a slave is present.

Pete McLean moved and Tom Hanan seconded that CSEL be changed to show device 1 at the end of the cable in ATA-3. The motion carried 7:2.

Dan Colegrove responded that his no vote was because the connector solution is preferable to modifying the cable since the connectors could be molded with end user labels and that having a single solution is preferable to having multiple solutions.

10.2 System Issues [Penman] ()

Duncan Penman proposed a redirection of the System Issues study group. Little has been accomplished in the last six months. The issues should be handled on a case by case basis within the appropriate group rather than by having a separate activity. The ATA ad hoc agreed to his recommendation.

Jim McGrath suggested that the ATA working group undertake a project to develop a standard that addresses the systems issues. The following topics were proposed:

Host Configuration Guidelines

IDE Bus Master Controller/PCI Interface
EDD > 8 GB BIOS OS
System Level Queuing and Overlap
Partition Sizes > 2 GB
System Level Error Recovery

11. Call for Patents

Gene Milligan requested that anyone aware of any patents required for the proposals be disclosed early in accordance with the ANSI patent policy. He also pointed out that IBM has made a blanket offer of any of their patents that may be required by the interface standards.

As noted in earlier minutes the Secure Mode proposal involves patents pointed out by Pete McLean and he stated that a letter has been submitted by Maxtor. He also mentioned an IBM patent and Dan Colegrove noted that document 94-125 contains the letter regarding the ANSI patent policy. Gene observed that he has not heard as yet what Compaq's response was to the patent letter from the X3T10 Chair John Lohmeyer.

12. Open Issues List

The list of open issues was reviewed as follows:
a) clearing of pending interrupts and how it relates to writing the command register or reading the status register.
b) when is DMA mode? see item g)
c) need to add concept of PIO transfers for register access (during DMA registers are not accessible) [data register > PIO; data port > DMA]
d) measurement of rise/fall time - ATA-3
e) an annex is needed on the logical impact of shared cables. (Landis)
f) does DRQ active protect the command block registers at the end of a data transfer? ATA-3
g) If DMARQ is deasserted within a tL, when can it be reasserted? (Frank Story issue).
h) What should the t2i timing be for MODE 0 Command Block Registers? ATA-3
i) SECURE MODE features - remove it or modify it? ATA-3.
j) READ/WRITE LONG Commands going to vendor specific. ATA-3
k) READ/WRITE MULTIPLE & SET MULTIPLE should be mandatory? ATA-3

The group agreed that issues d, f, h, I, j, and k should be addressed in ATA-3.

13. Action Items

30) Larry Lamers to post a proposal that the 16-byte command packet should be defined as a transfer of a SCSI CDB as defined in an ANSI standard or X3T10 working draft.
31) Curtis Stevens to prepare proposed flow charts for ATA-3.
32) Gene Milligan to follow-up with Compaq on the reported security patent.

14. Future Meeting Schedule

The ad hoc meetings are authorized by the plenary for a maximum of tow plenary meeting cycles. However meeting dates beyond that are blocked out for planning purposes to enable the dates should they be judged to be required by the plenary. In the event X3 authorizes the formation of a new technical committee no more than six per year of these blocked dates would be assigned for the plenary week. The group also discussed the need to minimize the number of meetings required to fit the needs of the industry.

September 19-22, 1995 at the Red Lion in San Jose, CA hosted by Quantum.
October 17-20, 1995 at the ??? in Irvine, CA hosted by Phoenix Technologies.
November 28-December 1, 1995 - at the WD facility in Irvine, CA hosted by Western Digital.
Proposed dates for 1996 are:
January 23-26, 1996

February 20-23, 1996
March 19-22, 1996
April 23-26, 1996
May 21-24, 1996
June 18-21, 1996
July 23-26, 1996
August 20-23, 1996
September 24-27, 1996
October 22-25, 1996
November 12-15, 1996
December 1996 - No Meeting

The starting time for the meetings is 9:00 am.

The meeting week agreed to by the ad hoc for the September meeting is:

	Tuesday	Wednesday	Thursday	Friday
9:00 am - 12:30 p.m.	ATAPI	ATA-3	ATA-3	ATA Futures
2:00 p.m. - 5:30 p.m.	ATAPI	ATA-3	ATA-3	ATA Futures

Note: The attendees may elect to have working lunch sessions on any of these days.

ATA Futures -
- cable annex (2 hours)
- overlap & queuing (2 hours)
- new projects (1 hour)
- other issues (2 hours)
- analog issues (2 hours)
- connector issues (brief report ~ 0 hours)

ATA-3
- ATA-3 issues
- document review

ATAPI
- ATAPI issues
- document review

15. Adjournment

The meeting adjourned Friday at 12:00 noon.