To: X3T10 SPI-2 Study Group

From: Bill Ham, Digital Equipment

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Subject: Proposal for SPI-2 electrical interface

1. Physical interconnect

1.1 Cable media

The same cable and interconnect media specified in SCSI-3 SPI and SCSI-3 FAST 20 shall be used for all interconnect.

1.2 Connectors

All the connectors specified in SCSI-2 and SCSI-3 SPI shall be allowed.

[Editor's note: Additional shielded device and cable connectors based on the VHDCI are expected to be submitted as proposals]

[Editor's note: Additional unshielded device and cable/backplane connectors based on the 80 pin SCA-2 connector are expected to be submitted as proposals]

2. Bus termination

2.1 Termination power

All bus terminators shall be powered from at least one source of termination power. The TERMPWR lines in the cable are available for distribution of termination power. Direct connection between the termination power source and the individual terminators without using the TERMPWR line is also allowed.

If the termination power source is connected to the cable TERMPWR line, the source shall be isolated in a manner that prevents sinking of current fron the TERMPWR line if the termination power source falls below the voltage existing on the TERMPWR line.

[Implementor's note: This requirement is frequently met by using diode isolation]

Termination power sources and the associated power distribution scheme used shall be capable of delivering adequate voltage and current to allow the terminator(s) to meet the requirements specified in SCSI-3 SPI under the designed application conditions.

[Implementor's note: Annex A provides guidance for the tradeoffs between terminator source voltage, terminator input requirements, wire gauge, bus width, and number of connectors in the TERMPWR path.]

The TERMPWR lines may be used for distribution of power for purposes other than for SCSI bus termination as long as the bus wiring and wire gauge comply with section xxxx and the voltage and current delivered to the SCSI bus terminators remain adequate to supply the requirements of the terminators.

2.2 Single ended bus termination

The single ended SCSI bus termination shall follow the specifications set forth in SCSI-3 SPI.

2.3 Low voltage differential bus termination

When operating in the low voltage differential mode SCSI bus termination specified in this section shall be used.

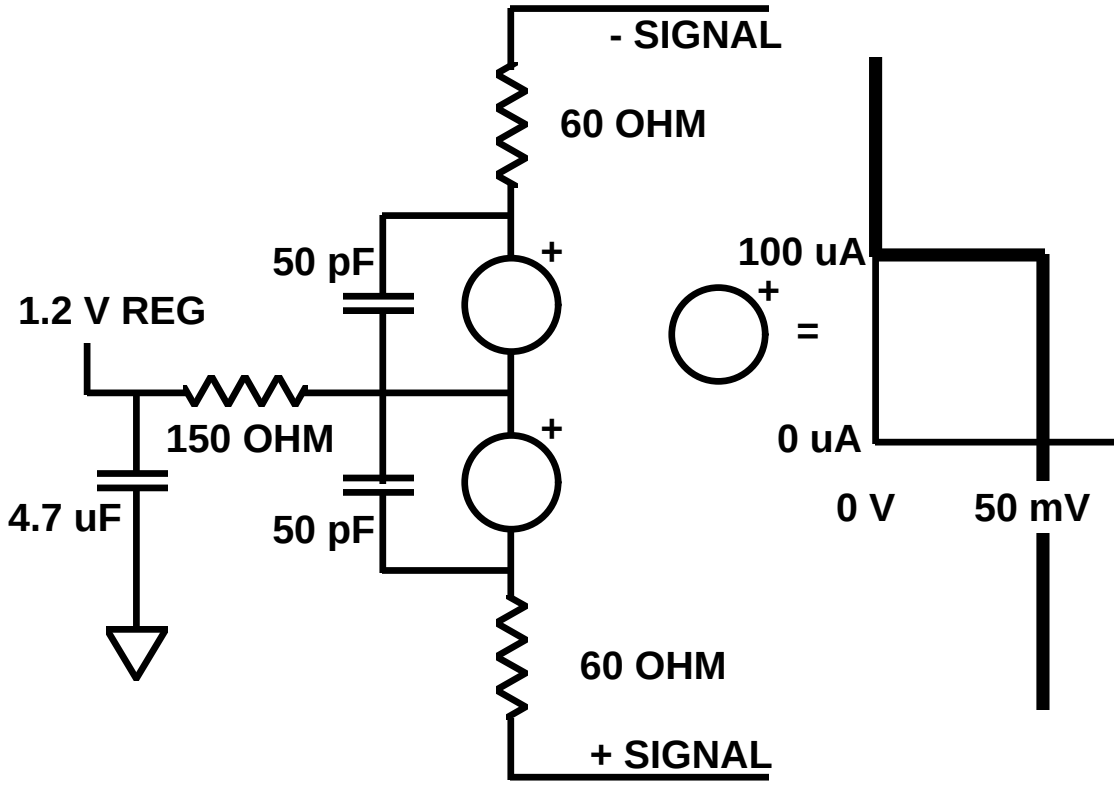


Figure 1 - LVDF terminator

Editor's note: need tolerances on components for terminator

3. Bus drivers and receivers

3.1 Single ended drivers

The single ended driver shall follow the specifications in SCSI-3 SPI and SCSI-3 FAST20. Single ended drivers are not specified for speeds higher than FAST 20.

3.2 Single ended receivers

Single ended receivers shall follow the specfications in SCSI-3 SPI and SCSI-3 FAST20. Single ended receivers are not specified for operation at speeds higher than FAST20.

3.3 Low voltage differential drivers

Low voltage differential drivers shall conform to the architecture specified in Figure 2. It is not required to implement the single ended drivers with the LV differential drivers but it is allowed to implement both LV differential drivers and single ended drivers in a single device.

The LV differential driver is a balanced current source that sources current to the - signal line and sinks current from the + signal line. The scheme produces dc differential levels of 180 to 240 mV with common mode level of nomically 1,25 volts when used withthe termnation scheme specified in section 2.

Drivers shall negate previously asserted signals for at least a bus settle delay prior to returning to the high impedance state. [This requirement is caused by the low bias current available from the terminators.]

LV differential drivers shall meet the specifications in Table 1.

Table 1 - LV differential driver operating specifications

Parameter	max	nominal	min	Notes
On current	4.0 mA	3.5 mA	3.0 mA	under bus operating conditions
Off current	10 uA			@SE Vin < 3.3V
off to on skew - signal to + signal	50 pS			
on to off skew - signal to + signal	50 pS			
| + signal on current - - signal on current|	500 uA			
common mode compliance voltage			±1.6 volts	

[Note: need detailed test conditions for drivers and slew rate specifications]

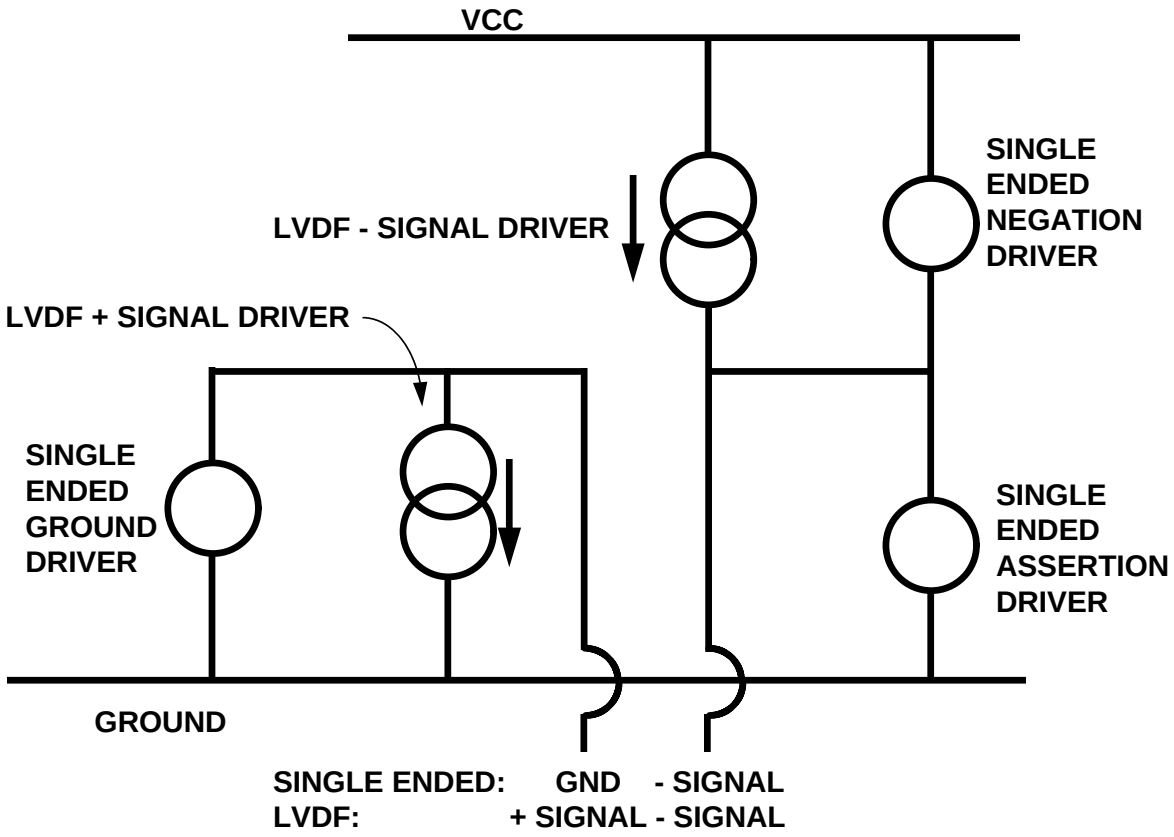


Figure 2 - Universal driver architecture

3.4 Low voltage differential receivers

Low voltage differential receivers shall meet the specifications in Table 2.

Table 2 - LV differential receiver operating specifications

Parameter	Maximum	Nominal	Minimum	Notes
Input voltage (dc single ended))	4.0			
input sensitivity (differential)			50 mV ????	
Input voltge (differential)	±3.3		0	
Common mode dc V	2.35		0.05	
input current (uA)	10			@0 to 4 V to local ground each input
input capacitance (pF)	15			each input to local ground

Implemenetor'snote: LV differential receivers will usually be implemented as shown in Figure 3.

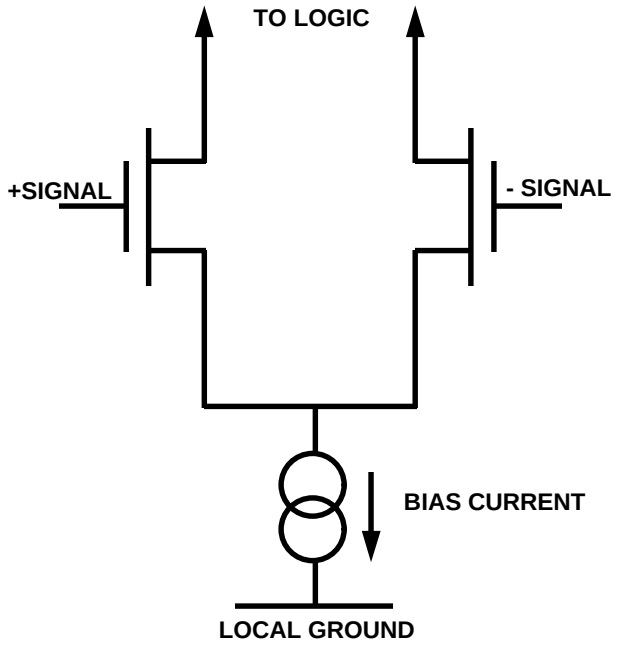


Figure 3 - LV receiver example

Receivers shall not detect differential input voltages near 0 as a third logic level. This requirement may be waived if the duration of the near 0 voltage is at least 250 mS.

Implementor's note: It may be desirable to use a long term near zero differential input level to detect fault ocnditions such as open connectors and missing terminators.

4. Transmission mode detection

4.1 LV DIFFSENS driver

The LV DIFFSENS driver sets a voltage level on the DIFSENS line that uniquely defines a LV differential transmission mode. All LV differential terminators shall provide a LV DIFFSENS driver according to the specifications in Table 3.

Table 3 - DIFFSENS driver specifications

Parameter	max	nominal	min	notes
output voltage se	1.4	1.3	1.2	
Output current dc	15 mA		5 mA	With TERMPWR @ operational levels
Input current dc	10 uA			With TERMPWR less than operational levels or with terminator disabled
Input current ac (Noise load)	0.35 mA			

4.2 LV DIFFSENSE receiver

All LV differential devices shall incorporate the LV DIFFSENSE receiver that detects the voltage level on the DIFFSENSE line for purposes of informing the device of the transmission mode being used by the bus. The LV differential receiver shall be capable of detecting single ended, LV differential, and HV differential modes. Table 4 defines the receiver input levels for each of the three modes.

Table 4 - DIFFSENS input levels

Mode	Single ended	HV differential	LV differential
DIFFSENS line	GROUND (< 0.5 V dc)	5V pull up through 1K (> 2.5 V dc)	0.7 to 1.9 V dc
All voltages measured at the device connector with respeot to local ground			

The LV DIFFSENS receiver shall incorporate low pass filtering equivalent to a 20K ohm resistor with a 0.1 uF capacitor to local ground. [This requirement provides ac common mode protection to the DIFFSENS function and allows ac receiver common mode levels much greater than 0.5 V.] LV DIFFSENS receivers shall provide 100 K ohms ±20% to local ground for purposes of providing ground refernece if no DIFFSENS drivers are connected to the bus.

A typical implementation of a LV DIFFSENS receiver is shown in Figure 4.

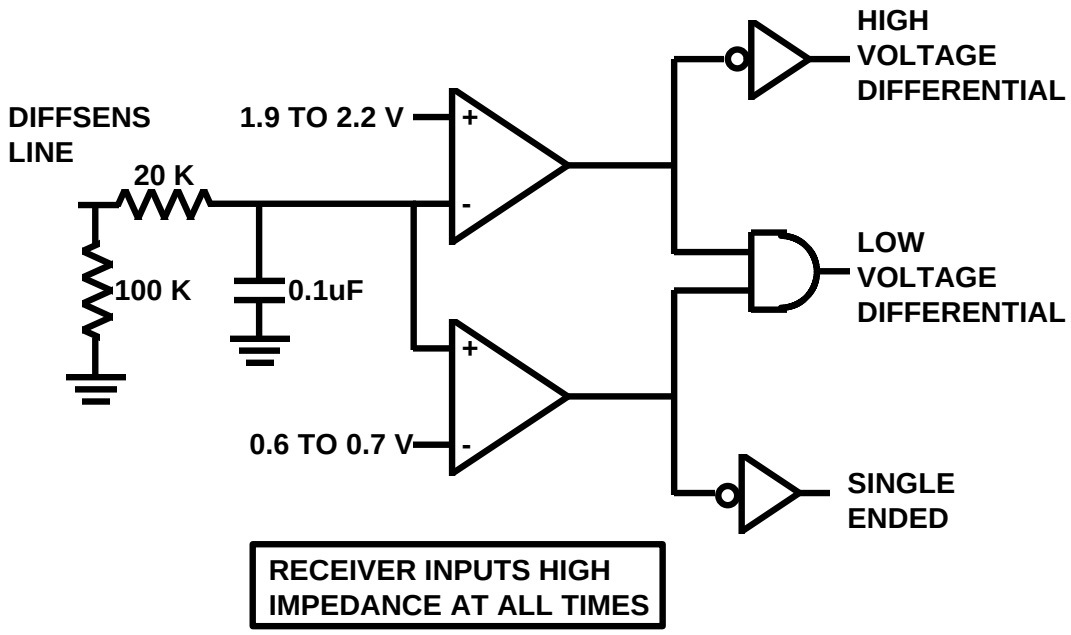


Figure 4 - LV DIFFSENS receiver

5. Contact assignments

Table 5 - Lov voltage differential contact assignments - P cable

Signal name	Connector contact number	Cable conductor number		Connector contact number	Signal name
+DB(12)	1	1	2	35	- DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
+DB(0)	6	11	12	40	-DB(0)
+DB(1)	7	13	14	41	-DB(1)
+DB(2)	8	15	16	42	-DB(2)
+DB(3)	9	17	18	43	-DB(3)
+DB(4)	10	19	20	44	-DB(4)
+DB(5)	11	21	22	45	-DB(5)
+DB(6)	12	23	24	46	-DB(6)
+DB(7)	13	25	26	47	-DB(7)
+DB(P)	14	27	28	48	-DB(P)
GROUND	15	29	30	49	GROUND
DIFFSENS	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
+ATN	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
+BSY	23	45	46	57	-BSY
+ACK	24	47	48	58	-ACK
-RST	25	49	50	59	-RST
+MSG	26	51	52	60	-MSG
+SEL	27	53	54	61	-SEL
+C/D	28	55	56	62	-C/D
+REQ	29	57	58	63	-REQ
+I/O	30	59	60	64	-I/O
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

6. LV diferential configuration rules

The overall distance between terminators shall be a maximum of 35 meters.

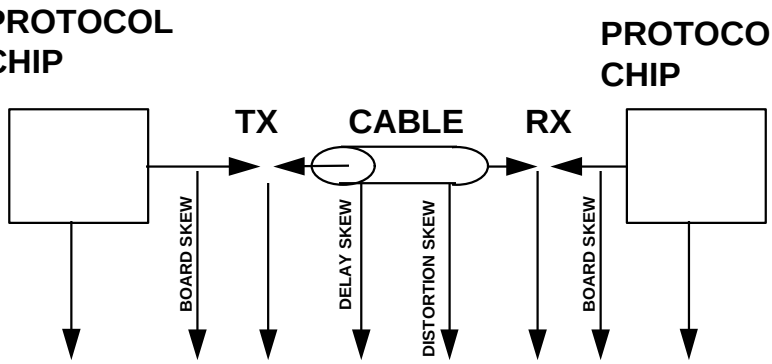
[The real length limits are likely to be determined by attenuation limits and are not known at this time.]

The difference in stub length for devices shall be less than 0.5 inches from the device conenctor to the bonding pad on the silicon chip for the REQ, ACK, DATA and PARITY signals..

The difference in capacitance to local ground between REQ, ACK,DATA, and PARITY signals on stubs shall be less than 5 pF at the device connector.

The skew between the + and - signal of any REQ, ACK, DATA, or PARITY stub shall be less than 5 pS.

SETUP AND HOLD TIMINGS



FAST									
10 SE	24	1.0	23	4.0	4.0	15	1.0	14	SETUP
	34		33			25		24	HOLD
10 DF	32	9*	23	4.0	4.0	15	10*	5	
	42		33			25		15	
20 SE	12	0.5	11.5	3.0	2.0	6.5	0.5	6	
	17		16.5			11.5		11	
20 DF	16	4.5*	11.5	3.0	2.0	6.5	5.5*	1	
	21		16.5			11.5		6	
40 SE/DF	5	0.25	4.75	1.5	2.0	1.25	0.25	1	
	9		8.75			5.25		5	
80 SE/DF	5	0.25	4.75	1.5	2.0	1.25	0.25	1	
	6.5		6.25			2.75		2.5	

* INCLUDES SEPARATE TRANSCEIVER SKEW