0.0.1. Multiword DMA Data Transfer

```
                     |<----------------- t0 ---------------->|                        >| tQ  |<
            ________________________________________________________                   |     |_________
 DMARQ  ___/                     |    \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\_________________/
             |                  >| tW |<                    |<--tL-->|            |
             |<----- tX -------->|    |                     |        |            |
              ___________________________________________________________________        _
 DMACK- ______/                                                                  \______________/
             |<-tI->|            |                          |        |   |
             |      |<-- tD ---->|<----------- tK -------->|      ->|tV |<--tJ-->|
             |      |            |                          |            |        |
 DIOR-       |      |____________|                          |____________|        |
 DIOW-  _____________/            \__________________________/            \________________________
             |      |            |                                                |
             |    ->| tE |<-     |                                                |<-tZ->|
 READ      ->| tY |<-     ________________                  ______________              |
 DD0-15 ----------<XXXXXXXX________________XXXXXXXXXXXXXXXXXXXXXXXXX______________XXXXXXX>-------
                         |       |        |
                         |<-tGr->|<--tF-->|
 WRITE                ______________________                    ____________________
 DD0-15 XXXXXXXXXXXXXXXX______________________XXXXXXXXXXXXXXXXXXXXXXX____________________XXXXXXXXX
                      |<--tGw--->|<---tH--->|
```

tV, tX, and tY are new timings for Synchronous DMA!

Figure 12 - Multiword DMA Data Transfer (Part 1 of 2)

Aggressive Timing for Faster PCI Systems:

	Multiword DMA timing parameters	Mode 2 nsec Min	Mode 2 nsec Max	Mode 3 nsec Min	Mode 3 nsec Max	PCI Clock 25 Mhz	PCI Clock 30 Mhz	PCI Clock 33 Mhz	Requires ***40***ns VLSI Access Times.
t0	Cycle time	120		60		80	66	60	60-***15***-5=***40***ns
tD	DIOR-/DIOW- 16-bit	70		25		35	28	25	
tE	DIOR- data access		---		---	---	---	---	
tF	DIOR- data hold	5		***0***		***0***	***0***	***0***	
tGr	DIOR- data setup	20	n/a	***20***		***20***	***20***	***20***	
tGw	DIOW- data setup	20		15		15	15	15	
tH	DIOW- data hold	10		5		5	5	5	
tI	DMACK- to DIOR-/DIOW- setup	0		0		0	0	0	
tJ	DIOR-/DIOW- to DMACK hold	5		5		5	5	5	
tKr	DIOR- negated pulse width	25		25		25	25	25	
tKw	DIOW- negated pulse width	25		25		25	25	25	
tLr	DIOR- to DMARQ delay		35		---	---	---	---	
tLw	DIOW- to DMARQ delay		35		---	---	---	---	
tQ	***DMACK- to DMARQ delay***	***---***		***0***		***0***		***0***	
tV	DMARQ neg to DIOR/DIOW neg		---	***20***		***20***	***20***	***20***	
tw	***DMARQ hold***	***---***		***0***		***0***	***0***	***0***	
tX	DMACK- to DIOR/DIOW neg			t0		t0	t0	t0	
tY	DMACK- to DD0:DD15 Low Z			5		5	5	5	
tZ	DMACK- to tristate		25		25	25	25	25	

The above Timing Diagrams and tables show that high speed operation with all of the popular PCI clock speeds will not be easy. The aggressive timings shown above provide a more even distribution of performance between the different PCI clocks. In order to achieve these aggressive timings WD feels that we must change to synchronous DMA. Changing to Synchronous DMA will require that we change our VLSI to meet the aggressive timings above. We feel that these timings are appropriate given the time frame for ATA-4 which should allow everyone to get these new modes into their new silicon.

The following issues were identified for the implementation of mode 3 Synchronous DMA:

- Synchronous DMA is needed to maintain achievable access time margins for host and drive VLSI.
- 4Ma drivers are needed to minimize cable settling time which has a direct impact on the access time required by the interface VLSI. 4ma should deliver settling times of about 20ns. If possible we should make further improvements to the cable configuration to reduce cable settling time from an estimated 20ns to 15ns.
- Input receiver hysterysis should be specified to minimize the impact that ringing and system noise have on settling time.
- Host and Drive VLSI should use edge vs sampled qualification of the rising and falling edges of DIOR and DIOW to eliminate clock related limitations on the pulse width of DIOR and DIOW.
- ***tGr is 20ns based on 15ns cable settling time and 5ns Host setup time.***