SPI-2 LVDS Driver Tests

Title: D:\UNITRODE\LVDF_1.EPS

Creator: GENERIC 6.0 CreationDate: 7/5/95 10:18:8 AM

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SPI-2 LVDS Driver Z

Title: D:\UNITRODE\LVDF_2.EPS

Creator: GENERIC 6.0

CreationDate: 7/5/95 9:12:11 AM

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SPI-2 LVDS Waveform

Title: D:\UNITRODE\LVDF_3.EPS

Creator: GENERIC 6.0

CreationDate: 6/30/95 3:17:49 PM

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SPI-2 LVDS Termination

Title: D:\UNITRODE\DIFSENS.EPS

Creator: GENERIC 6.0

CreationDate: 7/5/95 8:59:23 AM

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SPI-2 LVDS Diff Sense

Title: D:\UNITRODE\DIFSENSB.EPS

Creator: GENERIC 6.0

CreationDate: 7/5/95 9:5:32 AM

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SPI-2 LVDS Bus

Title: D:\UNITRODE\LVDIF-5A.EPS

Creator: GENERIC 6.0

CreationDate: 7/7/95 1:50:11 PM

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June 21, 1995 Merrimack MTG

- Reviewed the document sections of SPI that will be effected by LVDF SPI.
- Studied the Diff Sense issues and set new values
- Reviewed common mode issues with each interface
- Reviewed the cost objectives of LVDS
- Defined the pinning for the based on Single ended, regenerated table done in Harrisburg, but not documented.
- Note: FAST-40 single ended would still be a longer distance than ATA. This should be a viable standard.
- FAST-40 and FAST-80 will require very low delta stub and capacitance for data, parity, ack and req signals. The additive effect of 7 or 15 devices will exceed the skew budget.
- Worked timing issues for FAST-40 and FAST-80, external drivers and receivers can not be used, there is no margin in the skew budget.

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