SCSI SPI-2 Low Voltage Differential Signaling

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11-November-1995

1.0 Introduction:

The Low Voltage Differential Signaling (LVDS) specification, SP-3357 which will become EIA/TIA 644, is specified like EIA422 for a single driver with multiple receivers and the single driver is at one end of the bus. The SCSI Low Voltage differential standard will have to be like EIA485 where the driver and receiver can be any where on the bus. The driver power however must remain low. The Low Voltage differential is based on a current drive. The output current of the drivers must remain low, this requires adjusting the specification for termination on both ends of the bus with a differential characteristic impedance of 120 ohms and leaving a common mode impedance with a bias. The changes from the Low Voltage Differential standard will be in the voltages measured, the drive current will remain the similar to the SP-3357 specification. This will allow the drivers to be integrated into the controller maintaining the cost of low voltage differential in line with the single ended SPI implementations.

The receiver thresholds must be adjusted down from the SP-3357 specification to compensate for the lower drive voltage because of the termination on both ends of the line.

This is a second pass at adjusting the SP-3357 standard to the SCSI SPI-2 requirements. The basic 655 MBPS serial parameters appear to meet the longer term SPI goals of well over 100 megatransfer rates allowing for long term migration strategy for parallel SCSI. The initial version of the standard is being written for FAST-40 and FAST-80, future versions could include FAST-160 and FAST-320, over 320 megatransfer rates Skews may not be manageable. This should carry SPI through the year 2000, after 2000 FPI migration would be the logical strategy when the industry requires over 640 megabytes per second parallel fiber optics will most likely be the best migration path.

The high speed standard requires several new physical limitations, as the speed increases the skews become much more important. It is important to design the new standard for future migration increasing the speed. This requires line to line matching of drivers, receivers, capacitance and stub lengths to minimize the skew. Delta are more important than the physical delay time. The delta stub and capacitance difference between lines is most important on the devices, where there can be up to 15 devices of the same design on a single bus.

It is the intent that controllers will be built that can drive both low voltage differential and single ended depending on the bus configuration for the first generation. If all of the devices are low voltage differential then the system will run on low voltage differential, but if one or more devices or any system component is single ended then all the devices revert back to single ended. This will allow backward compatibility with the forward migration path for the first generation of low voltage differential. This document only deals with low voltage differential electrical levels and how to determine if the type of bus the device is attached to.

The devices for FAST-80 and higher may only be LVDS, not supporting the single ended devices.

The distance goal is 12 meters for FAST-40 & FAST-80. Testing will have to be done to insure adequate margin for 12 meters with 7 to 15 different bus loads.

1.1 Index

2.0 Basic Driver Concepts and Requirements

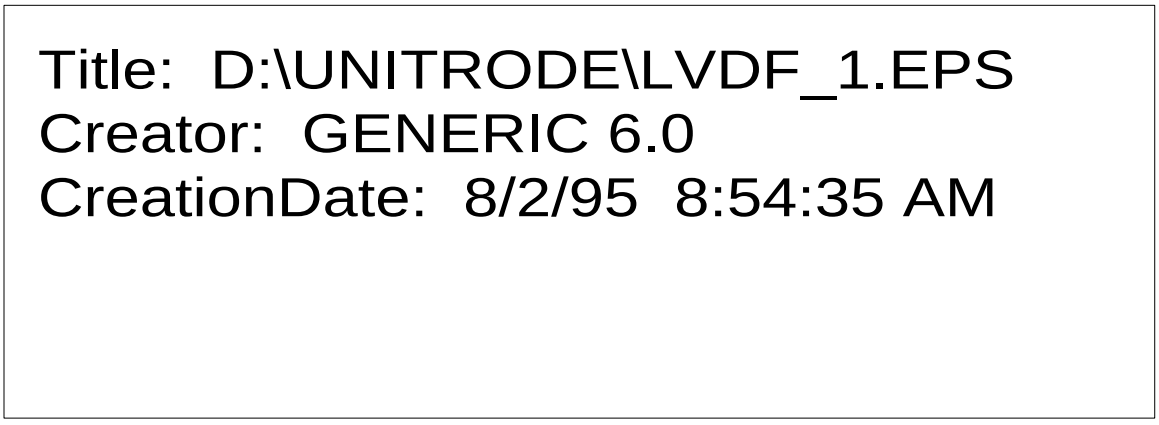
The low voltage differential driver is required to have a high degree of balance to minimize distortion and radiation. The driver is current based with a drive current range of 4.4 to 6.0 mA (May be increased to 5 mA with no upper limit) into a 60 ohm load with a common mode termination of 75 ohms to 1.25 Volts. This will produce a static signal of 264 to 360 mV with a common mode voltage of 1.25 volts. The low common mode will allow migration to lower voltage logic families, 3.3 Volts and 2.5 Volts.

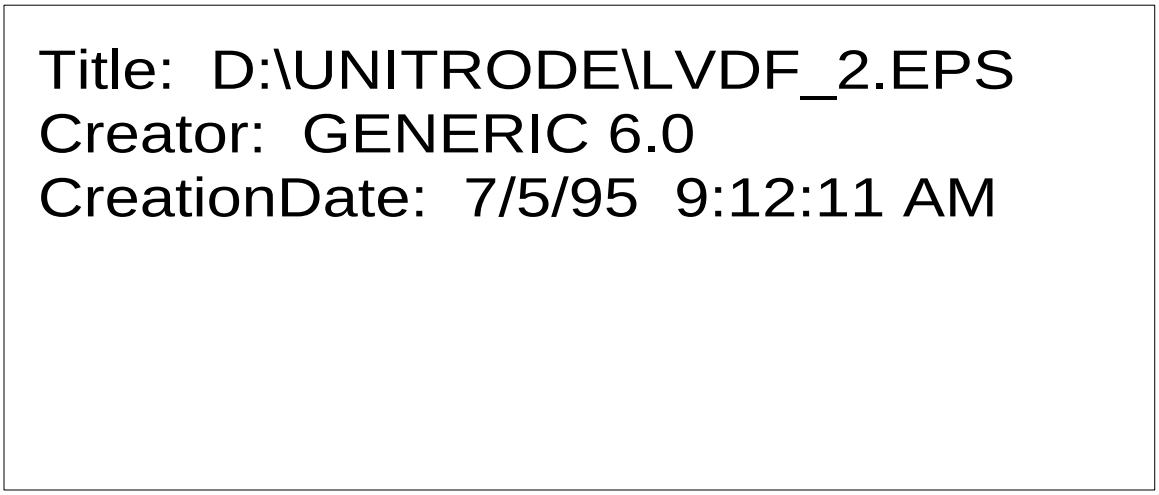
The drivers shall drive the bus to the failsafe state for one round trip time of the bus before tristating. Note: The terminators only provide a low current bias, the time to pull the bus to the failsafe state with the terminators would be too long with the terminator current restrictions. One round trip time for 12 meters would be 120 ns. The terminators only hold the line with a low bias current to the bias (failsafe) state.

2.1 Driver Characteristics

The driver output voltage is measured with two 30 ohm resistors in series load and a 75 ohm common mode termination to 1.25 Volts, the differential output voltage shall be 264 to 360 mV. The Output state will match the normal communications standards with the VA-VB voltage of -264 to -360 mV for a 1 state and +264 to +360 mV for a 0 State, with a maximum delta of 30 mV. The common mode voltage shall be 1.125 to 1.275 Volts with a maximum delta of 30 mV.

The driver open circuit output voltage VA-VB open circuit voltage may be close to the supply voltages. The standard does not restrict the voltage other than it shall be less than the supply voltages, 3.6 Volts Maximum.





2.2 Driver Short Circuit Measurements

Shorting the driver to ground the output current shall not exceed 24 mA in either state.

Shorting the differential driver output the current shall not exceed 12 mA in either state.

2.3 Driver Tristate Line Load Test

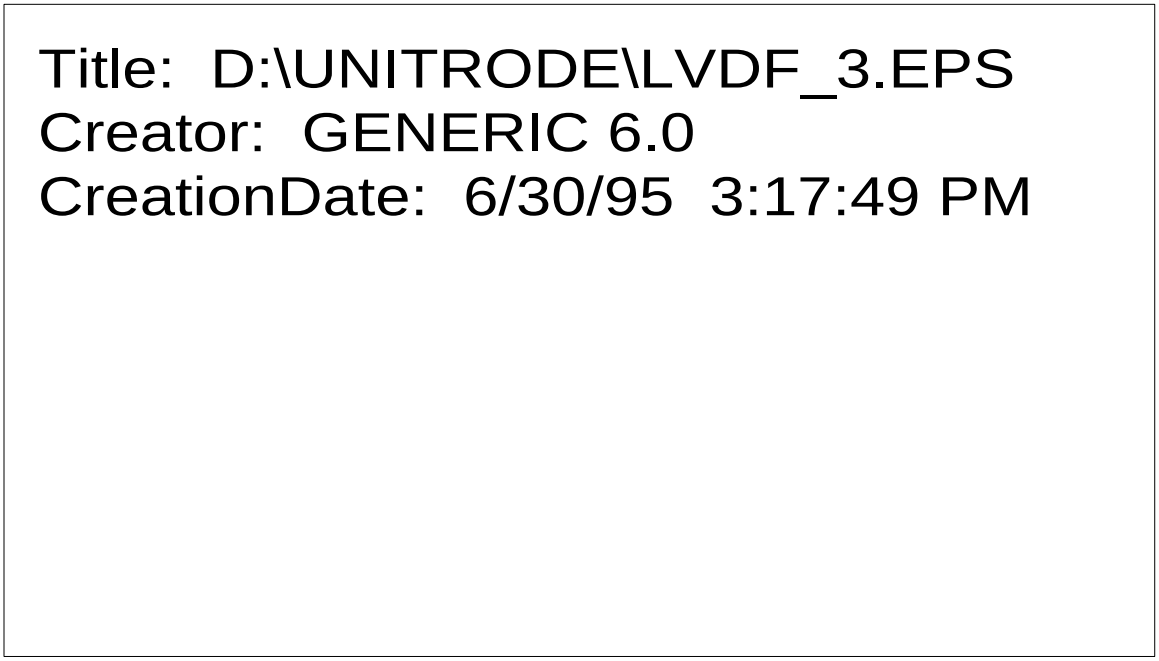
The SCSI SPI-2 applications combines the driver and receiver, the load for the driver and receiver combination see the receiver section 3.1

2.4 Driver Output Signal Waveform and Balance
The output signal wave form shall be measured with two 30 ohm resistors in series with a 5 pF differential Cl.

The rise and fall time is measured at the 20 and 80% points of the steady state voltage, Vss. The rise and fall time shall be 0.5 to 1.5 ns. (Note this fixes the rise and fall time to allow maximum future migration by only adjusting the timing.)

The overshoot and ringing shall be less than 20% of Vss.

The common mode dynamic imbalance, delta VOS shall be less than 100 mV.



3.0 Receiver Characteristics

The receiver shall operate over a common mode range of +0.05 to 2.35 Volts with a running speed maximum differential threshold of +/-70 mV. The maximum differential receiver input voltage may be as high as the 3.6 Volt supplies. The maximum receiver input voltage with respect to ground shall not be greater than 2.4 volts or less than ground. The receiver input impedance shall be high reducing the loading effects.

3.1 Transceiver load characteristics

The transceiver input current shall be less than 20 μA from 0 to 2.4 Volts when the other I/O pin is held at 1.2 Volts +/- 50 mV. Total device capacitance including etch and connectors shall be less than 15 pF, measured in single ended mode, as specified in SPI.

(Leakage was increased from 10 to 20 uA from silicon manufactures requested because 2.5 & 3.3 Volt logic less than .5 micron 10 uAs is impossible.)

3.2 Receiver Failsafing

ACK, REQ, BSY and RESET receiver failsafing is recommended for Open or Shorted cable, and a bus without termination/termpwr applied. The receiver may detect a bus failsafe state when the voltage remains below 50 mV levels for an extended period of time. The suggested time is 1 μs for the extended time period.

4.0 Termination

There shall only be two terminators enabled, one at each end of the bus.

The termination shall provide the differential and common mode termination with failsafe biasing. The termination shall be low power with a low idle current of less than 30 mA for 27 differential lines, a resistor divider network is not allowed.

(More drive current and reduced terminator complexity will change the terminator spec.)

The differential termination shall be 70 < 80 ohms with a bias voltage of 100 to 130 mV, low current 220 to 250 μA in the failsafe state. The line Asserted state the bias generator acts like an ideal forward bias diode and must handle at least 35 mA. The line negated state the bias generator acts line a zener diode, when more than 150 mV signal is applied it limits the voltage across the bias generator with a minimum of 4 mA current capability. The current must be limited to not effect the signal integrity with the low current drivers. Electrically when the bus is driven the termination looks like 70 < 80 Ohms differential and 150 ohms to 1.25 Volts.

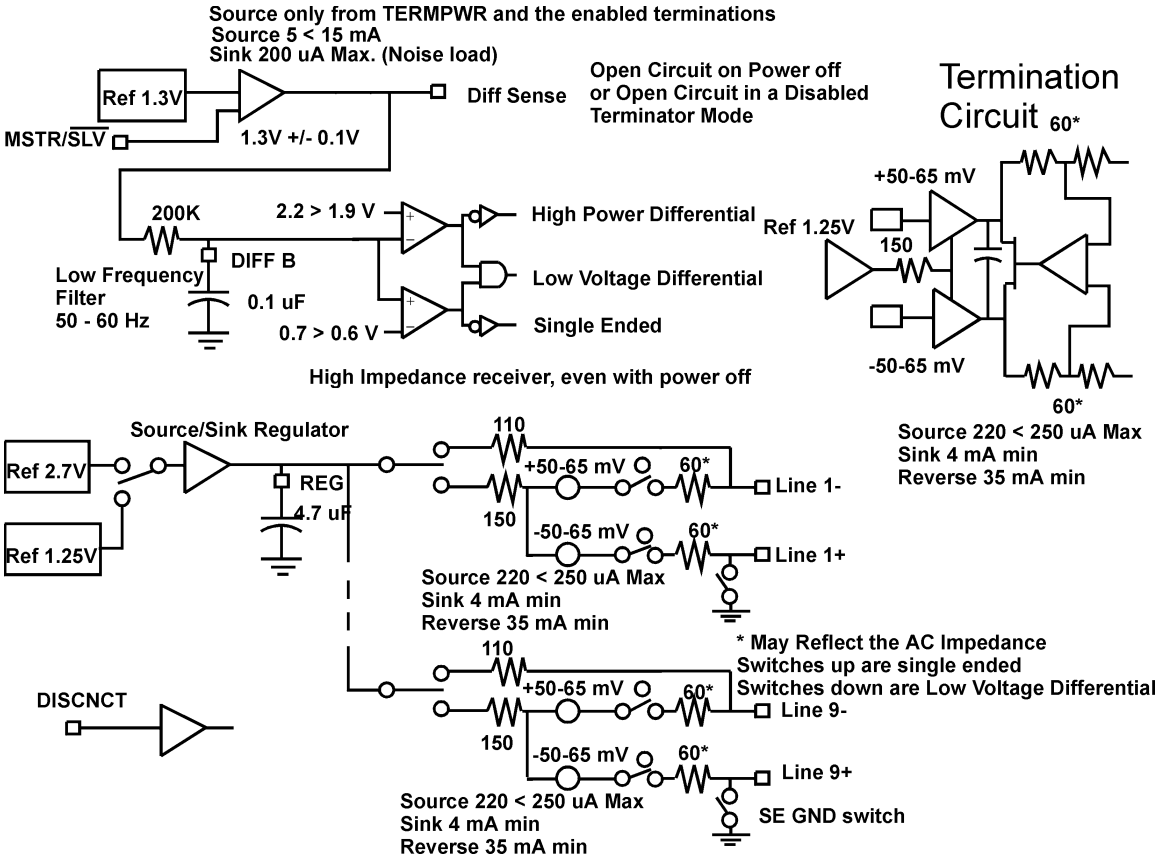
The ideal zener is built using a FET clamp circuit for the forward bias. When the terminator detects the line driven in the reverse direction it clamps the bias generators with the FET, the FET will handle the full 35 mA possible for SCAM arbirtation when it is possible to have all the drivers turned on. The bias generators are light source, heavy sink. The light source bias the line with 220 to 250 uA of current, but when the line is driven it becomes a heavy sink, 4 mA plus more than the maximum drive current..

The 40 - 80 pF capacitor across the bias generator/clamp is to respond to the high speed switching of the line, the clamp and bias generators need about 5 ns to respond to the line transients.

The common mode termination shall be 150 ohms +/-10% with a bias voltage of 1.25 Volts +/- 50 mV.

Note: A resistor divider network like the one used in high power differential SCSI would force an overall bias to the signal when the low current drive signals of LVDS are used. This would reduce the signal length that could be achieved by LVDS and would be a constant load on the TERMPWR line.

It is the intent for SCSI LVDS to be as low of power as possible and and robust as possible. This will give the user the best cost performance standard for disk connection. This makes the terminator more complex but improves the system margin and reduces the terminator power, which is a constant. Battery systems can not afford a high terminator idle current.


Source only from TERMPWR and the enabled terminations
Source 5 < 15 mA
Sink 200 uA Max. (Noise load)
Ref 1.3V
MSTR/SLV
1.3V +/- 0.1V
Diff Sense
Open Circuit on Power off
or Open Circuit in a Disabled
Terminator Mode
Termination
Circuit 60*
+50-65 mV
Ref 1.25V
150
-50-65 mV
60*
200K
2.2 > 1.9 V
High Power Differential
DIFF B
Low Frequency
Filter
50 - 60 Hz
0.1 uF
Low Voltage Differential
0.7 > 0.6 V
Single Ended
High Impedance receiver, even with power off
Source/Sink Regulator
Ref 2.7V
Ref 1.25V
REG
4.7 uF
110
+50-65 mV
60*
Line 1-
150
-50-65 mV
60*
Line 1+
Source 220 < 250 uA Max
Sink 4 mA min
Reverse 35 mA min
Source 220 < 250 uA Max
Sink 4 mA min
Reverse 35 mA min
* May Reflect the AC Impedance
Switches up are single ended
Switches down are Low Voltage Differential
DISCNCT
110
+50-65 mV
60*
Line 9-
150
-50-65 mV
60*
Line 9+
SE GND switch
Source 220 < 250 uA Max
Sink 4 mA min
Reverse 35 mA min

4.1 Diff Sense

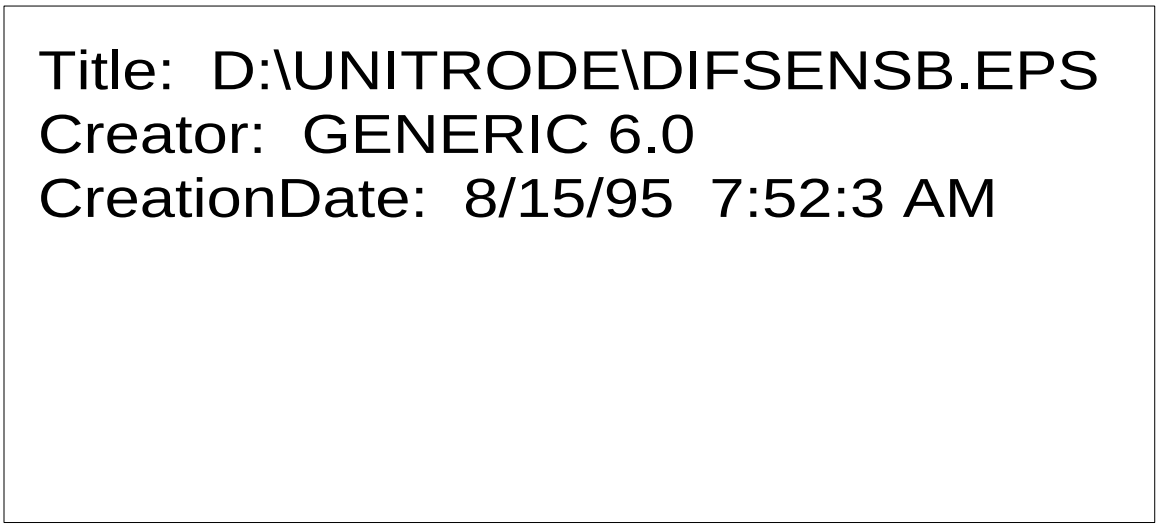
Only the enabled terminators at the end of the bus shall provide a bias current to the differential sense line 1.3 Volts +/-0.1V sourcing 5 to 15 mA, Sinking 200 μA Max.

Circuits for the diff sense detection shall filter out noise with a 20K ohm series resistor and a 0.1 μF capacitor. Below 0.6 volts shall be detected as single ended, 0.7 to 1.9 Volts shall be detected as low voltage differential, above 2.2 Volts shall be detected has EIA485 standard differential SCSI.

A 200K ohm pulldown resistor on the input of Diff Sense for open circuit condition.

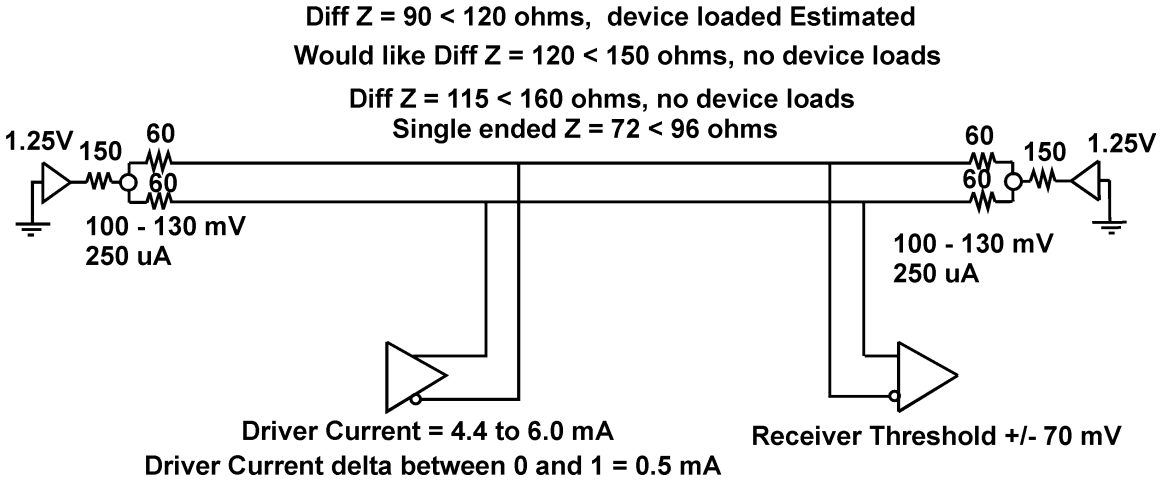
When the terminator detects single ended, and has the capability to terminate the single ended line. The Positive line will be connected driven to ground and the negative line will revert to the standard single ended termination as defined in FAST-20.

When the terminator detects High power - EIA485 type devices it will shut down. High powered differential uses a different pinout, and can have very high common mode voltages. (May need to be reviewed for a better option ?)



5.0 Bus view of the System

The overall system allows for a DC common mode voltage of +/- 0.6 Volts, but allows an AC common mode of +/- 1.2 Volts above 40 Hz. The receivers and drivers will allow for 0 to 2.4 Volts maximum voltage range in reference to ground.



5.1 System SKEW Issues

The higher speed operation requires skew to be reduce on the devices and controllers. The skew for devices can add up when up to 15 devices of the same type are used on the sample bus, each device will delta skew will add. The delta etch and package length of signal lines on a device or target shall be less than 0.5 inches. The delta capacitance shall be less than 5 pF.

The delta skew within a differential pair shall be less the 25 ps.

6.0 Power Budget

A key goal is to design a interface that transceivers can be incorporated into the controller chip, to do this the power must be limited in the transceivers to about 500 mWatts. The transceivers incorporated in the controller drastically effect the skew budget, allowing for much higher speed operation.

The power table was developed in the July & August meetings.

- **Transceiver power calculations for a 27 line device at 3.3 Volts + 10%.**
- **Maximum 21 Active Drivers on a 27 line device.**
- **6 Active Receivers**
- **Driver control current 1 mA * 3.6 Volts, 3.6 mW * 21 Lines = 75.6 mW**
- **Driver power 6 mA * (3.6-.36) Volts, 19.44 mW * 21 Lines = 408.24 mW**
- **Receiver Power 2.5 mA * 3.6 Volts, 9 mW * 6 Lines = 54 mW**

Total Transceiver current 537.84 mW

7.0 Slides

8.0 History

8.0 SPI-2 and EPI History Document

The Future Direction of SCSI Parallel
Why SCSI Parallel LVDS?

Paul D. Aloisi
Unitrode
October 1995

Introduction:

The SCSI parallel committee has been reactionary, after a need develops, it starts working on a new version of the standard. The committee has watched many of the spin off groups, SSA, Fiber Channel and ATA, from the SCSI/Computer storage bus committee form their own committee with a much more forward looking approaches. The spin off groups have both a technical committee and a marketing group to promote the standard. The marketing groups publish articles and have rooms at the major shows to promote the standard. Parallel SCSI is a closet standard, only a few of the companies advertise the direction of parallel SCSI, most users and systems people don't find out about advances until the hardware is available.

Fast-20 the last SCSI parallel document was finished in record time. SCSI-2 had taken 5 years, SCSI-3 - SPI had taken 3 years, Fast-20 had taken 18 months. The FAST-20 document has several issues that involved physical limitations, the bus length for single ended was too short, and the number of devices was too limited, the differential SCSI requires too much of the skew budget for the transceivers and the transceivers are a significant cost burden.

Is FAST-20 the last parallel specification and Serial or Fiber Channel takes over?

What Performance is needed for the future? Have SSA and Fiber Channel selected the right performance and price for the future? Where does IDE/ATA go? IDE/ATA is at its performance limit for its technology.

The future disk sizes and performance requirements were mapped out through the year 2000. There are 20 and 30 Gigabyte drives in design, by 2000 200 Gigabyte to 1 Terabyte drives will be available. The 40 Megabyte transfer rate of today will be 400 Megabyte transfer rate by 2000 going to over a Gigabyte per second in the early 2000 time frame. SSA can never run the performance required after 100 Megabytes per second it is at the maximum physical limit.

Fiber Channel comes at a high cost with some basic performance limits, the next speed increments come at a high cost, 1 gigabit fiber channel can still be done in silicon, when the speed increases to 4 gigabit GaAs is required. The cost go up very fast with the higher speeds.

Both SSA and Fiber channel require new drivers and the interconnect system is new to the users. Old SCSI devices do not work on either system, Systems in many instances have to support two buses, the old parallel for the legacy devices and the new bus for new devices.

Strategy

The committee set out a performance level goal, both speed, distance, and number of devices. The speed needs to go well beyond 100 megatransfers per second or 200 megabytes per second. The distance should be at least 10 meters. 16 devices per bus segment.

Secondary goals were to keep the same physical plant for migration, develop a low cost interface with the transceivers in the controller chip, and a high speed interface that would not be a major RFI problem. A power limitation was set of 600 mW maximum for the transceivers, this allows about 500 mW for the controller logic in the typical package used for SCSI controllers.

No new software drivers required, only minor changes to the current drivers for the higher speeds.

Migration or interim components should be developed that would work in the current single ended mode and work in the new mode when the bus had all new devices.

The bus pinning is different for single ended SCSI and differential SCSI, the new standard should be based on the single ended pinning to allow an easy migration from the current high volume application. (Note: differential SCSI is only about 5% of the SCSI market.)

Selection

The search was on to find a standard that could be adapted for SCSI parallel operation. Calls went out to IEEE representative and EIA/TIA representatives for standards in development that might meet the needs of SCSI Parallel.

EIA/TIA TR30.2 committee was developing a Low Voltage Differential Signaling standard (LVDS), Proposal PN3357 which was adopted as EIA/TIA-644 in August 1995. This is a point to point high speed, low voltage version of EIA 422B. After a short study period it was found that it could be converted to a multidrop standard easily and would easily meet the speed requirements with a maximum parallel estimate of 655 megatransfers per second as an upper limit.

The LVDS technology is a forward looking standard designed with a center point for 2.5 Volt logic, allowing future migration to low voltage technology. The new designs are 3.3 Volts, but by 2000 the standard voltage of 2.5 Volts is likely. The power is low enough to integrate the transceivers into the controller chip.

Development

X3T10-95/0269 document was developed in the X3T10 committee based on the EIA/TIA PN3357 document. The drive current, receiver thresholds and termination had to be modified for the multidrop application. Converting Point to Point to Multidrop the major effect is on the signal levels and drive. The line is terminated on both ends instead of just the far end. The drive scheme is based on current mode drivers to simplify the drive circuits for easier integration into the controller chip. The current goes out from the driver in two directions effectively cutting the signal level in half. The signal levels are effectively the current through the signal line times the impedance at that point in the cable, devices attached to the cable low the effective impedance of the cable.

The multidrop drivers must tristate with very low leakage to allow several drivers to share the same bus. The termination at each end of the line is 120 ohms and the SCSI differential cable impedance is 115 to 160 ohms differential. The drivers see the termination at a DC state, during transfers they see only the cable impedance. The cable impedance Is reduced when devices are connected to the bus. A loaded bus the cable impedance would be in the range of 90 to 120 ohms.

The controllers a mainly a digital technology, the analog requirements must be kept to a minimum. The only true analog components on the bus are the active terminators. All precision requirements are placed in the terminators keep the controller cost to a minimum. The maximum power that the controllers could handle for the transceivers is 500 mW, at the very maximum 600 mW. The power limit dictates the maximum driver current, establishing the basic limits.

The driver design working with the termination was simplified to a current mode drive. The termination sets the common mode reference point, differential 120 ohm termination and common mode 150 ohm termination to 1.25 Volts. The driver is a balanced differential current mode drive that reduces RFI by balancing the energy between the two signal lines. The maximum power limited the drive current to 6 mA maximum, a lower limit of 4.4 mA was chosen as a range that could yield very well without trimming in the controller technology.

The receiver thresholds are limited by the signal available and the noise margin. The receivers must detect +/- 70 mV signals. The receivers failsafing is an issue, this was not possible in most of the controller technology. The failsafe bias was pushed into the terminator similar to the requirements in the standard SCSI differential currently in SCSI-3 SPI.

The pinning is based on the single ended, but uses the diff sense line from the differential standard to determine the type of bus the unit is connected to. The active terminators set the bias of the diff sense line to 1.3 Volts, a current differential SCSI device pulls the line high with a diode an 1K resistor to +5 Volts. The single ended devices ground the pin. The devices on the bus is a LVDS when the voltage on the Diff Sense line is between 0.7 and 2.2 Volts. If one device is single ended the bus must run in single ended mode because the positive side of the differential pair is grounded. When single ended is detected all the devices ground the positive line of the differential pair. If a standard SCSI differential device is detected the all devices and the terminators turn off, shutting down the bus for several reasons.

The termination is similar to the high power SCSI differential termination, establishing the bias to the line when there are no drivers actively driving the line holding the bus at a known state.

The signal budget is tight to add more margin the bias is removed when the signal drives negative by an active clamp circuit - Ideal zener. The termination for the first generation will be both LVDS and Single ended. The disk drive companies only want to build one SCSI drive that can be used on the LVDS or automatically switch to single ended. The termination must switch with the drives. When a single ended device is connected to the bus it grounds the diff sense lines, the devices detect the single ended device from the diff sense line going below 0.7 Volts. All the devices turn on the ground drivers on the positive signal line and use single ended drive on the negative line. The speed is reduced to a maximum of Fast-20 in single ended mode. This allows the first few generations of LVDS devices to be backward compatible with the single ended devices. Bridges are being developed that will bridge single ended buses to LVDS buses, this will allow the controllers and high speed devices to run in LVDS mode and any older single ended devices will be after the bridge in single ended mode. The LVDS bus runs at the higher speed (Fast-40/Fast-80) and the single ended bus is limited to Fast-20. When the device is selected the speed is negotiated at the maximum speed of the single ended device.

The initial testing prove the basic length can be met, 12 meters with 16 devices and 25 meters point to point with speeds up to 100 megatransfers. It appears the length will have to be reduced at speeds over 100 megatransfers. The basic signaling test up at 200 megatransfers with reduce lengths appear to be within reasons.

Additional work is in development with options for wider buses (32 bit), very high density connectors, Enhanced Parallel Interface (EPI) document which includes low voltage, low power, hot plugging, point to point connections with distance in the 20 meter distances, bridges allowing the use of LUN addresses to expand the number of devices on a single bus from 15 devices to 15 devices attached to each device on the primary bus or 15 * 15 or 225 devices.

It appears at this time the maximum transfer rate will be about 300 megatransfers per second, with a 32 bit bus this is a 1.2 Gigabyte per second transfer rate.

Advantages

The advantages over the current Single Ended is much higher speeds, longer cable length, and more devices.

The advantage over differential SCSI is the reduce cost from integrating the transceivers into the controllers, and significantly higher speeds with a lower skew budget.

The advantages over SSA, much higher speed capability each of the paralleled lines can run the same speed as the single serial line. LVDS combine with EPI (Enhanced Parallel Interface) a large number of drives to be connected to a single bus. The LVDS balanced drive is a better drive scheme than the scheme for SSA. The only disadvantage is a 12 meter maximum loaded bus length. The 12 meters is adequate for most disk farms

The advantages over Fiber Channel lower cost, a more familiar cabling scheme, and higher speed per cost. The 600 megabyte per second maximum transfer rate possible with LVDS 16 bit bus is over a 5 Gigabit per second transfer which requires GaAS drivers and very expensive laser diodes and photodiodes. The 1.2 Gigabyte per second maximum transfer rate possible with LVDS 32 bit bus or over a 10 gigabit per second transfer rate from serial interface. Only very expensive telecom fiber optics runs at 10 gigabits per second now, it is not clear what the cost will be in the 2000 time frame.

Time Line

The March -95 X3T10 SCSI Working Group meeting, was the first meeting that starting looking forward to what needed to be developed as a standard to Parallel SCSI as a viable standard for the future. Working group meetings in April, May, and June reviewed the options, selected the basic interface. July SPI-2 Working Group LVDS X3T10-95/0269 was presented to the group as a working document to define LVDS.

Working group meetings in August lead to silicon design starts the first of September. Working groups continue to meet to work out the on going issues.

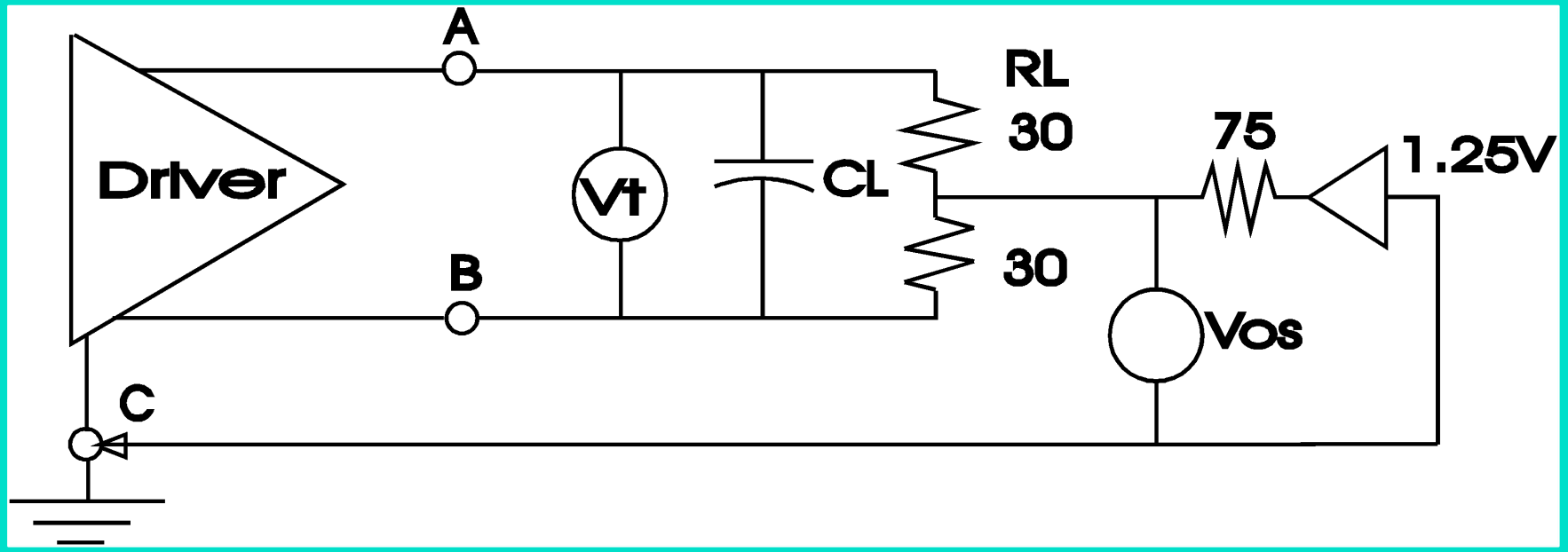
Sample silicon is due in April 96 time frame from several companies, with production parts scheduled for Summer 96. There will be several devices shown at COMDEX 96.

Summary

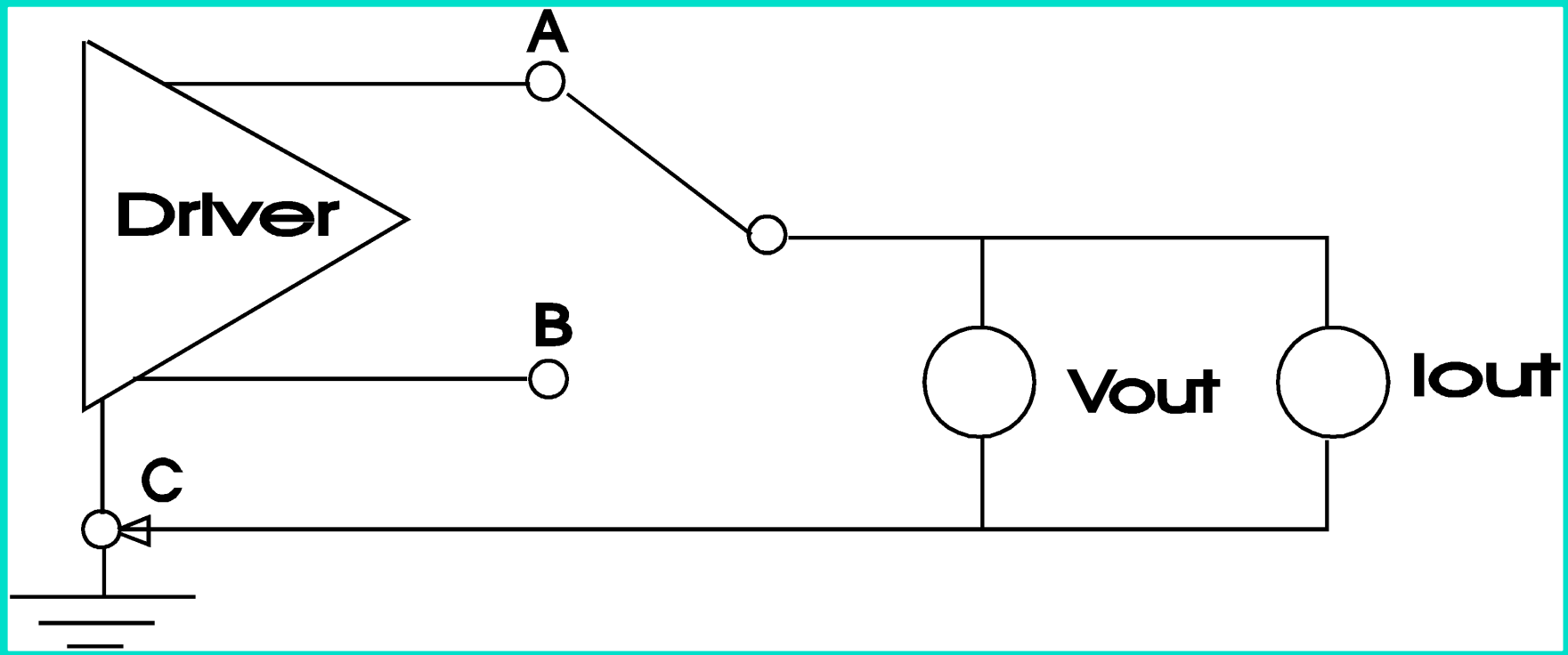
The death of parallel SCSI announced by several other technologies is very premature. The performance path for parallel SCSI leads it well beyond performance path of SSA, past fiber channel 2 at 4 Giga bits second.

Parallel SCSI has a migration path well past the year 2000 with performance that will out run the interfaces that claim to be the next generation interface.

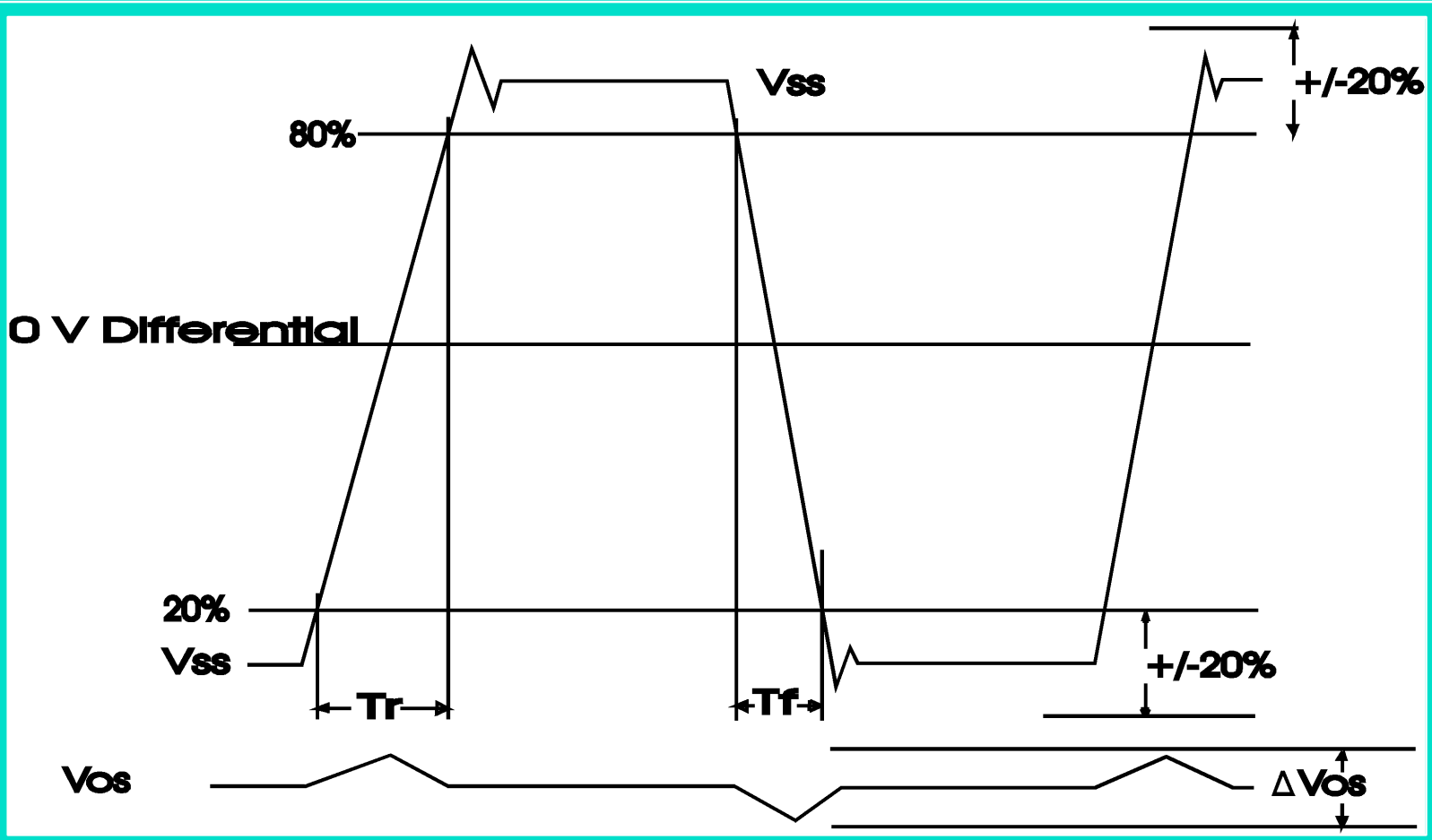
SPI-2 LVDS Driver Tests



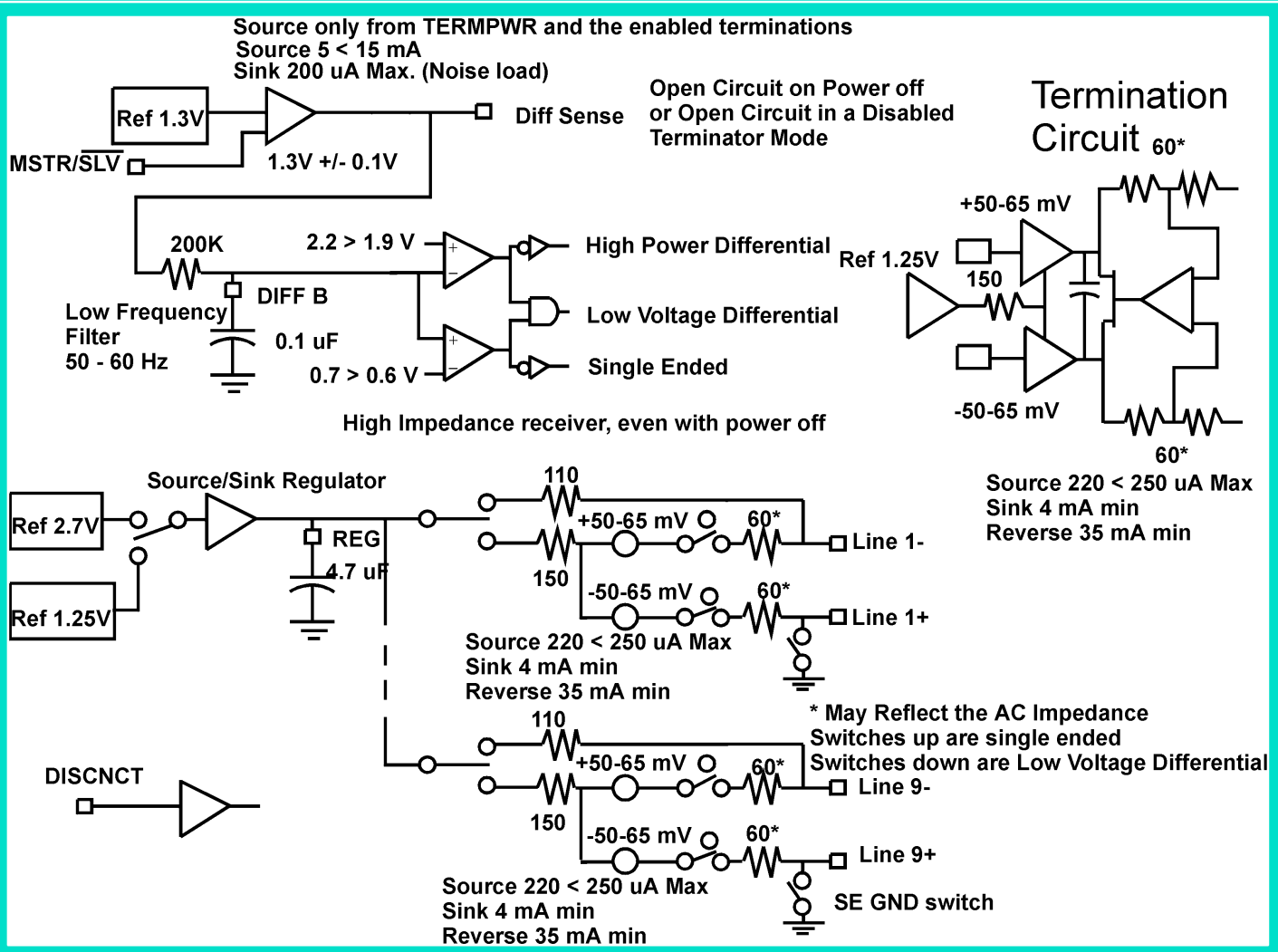
SPI-2 LVDS Driver Z



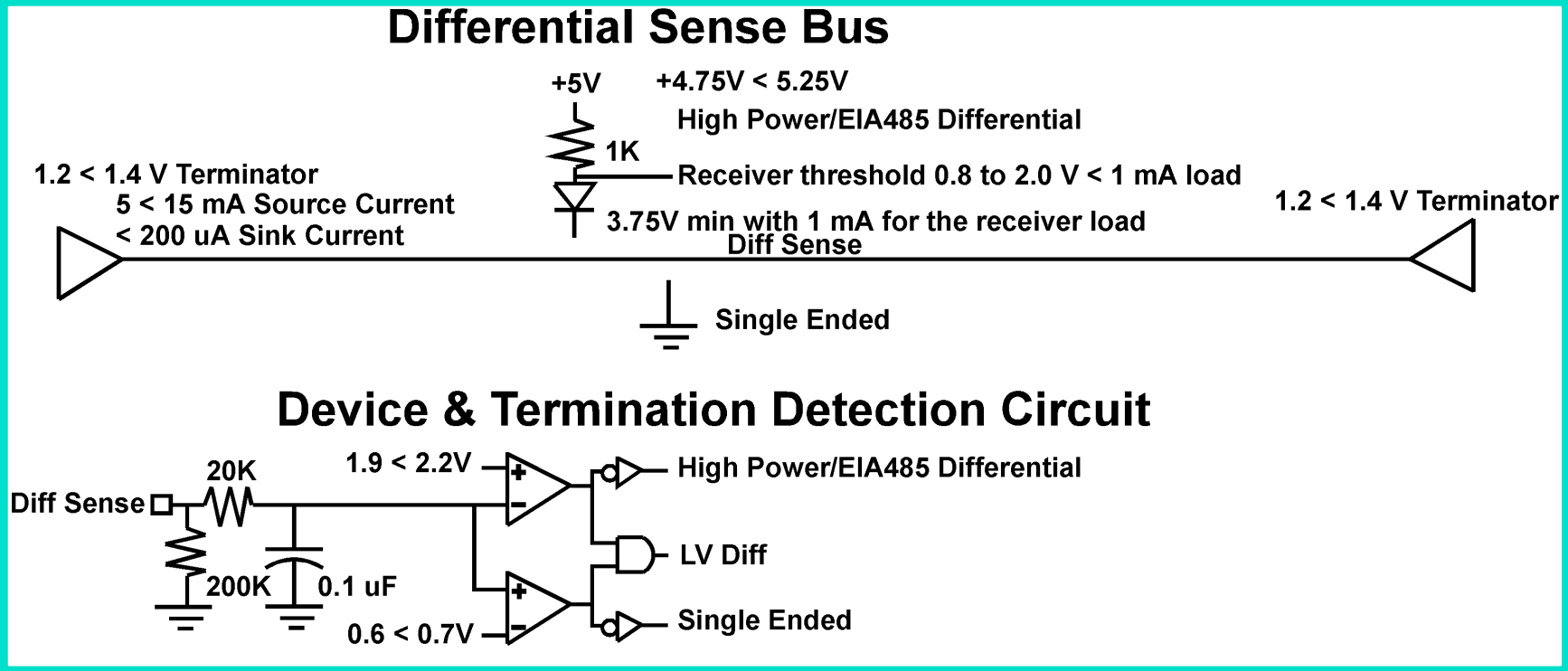
SPI-2 LVDS Waveform



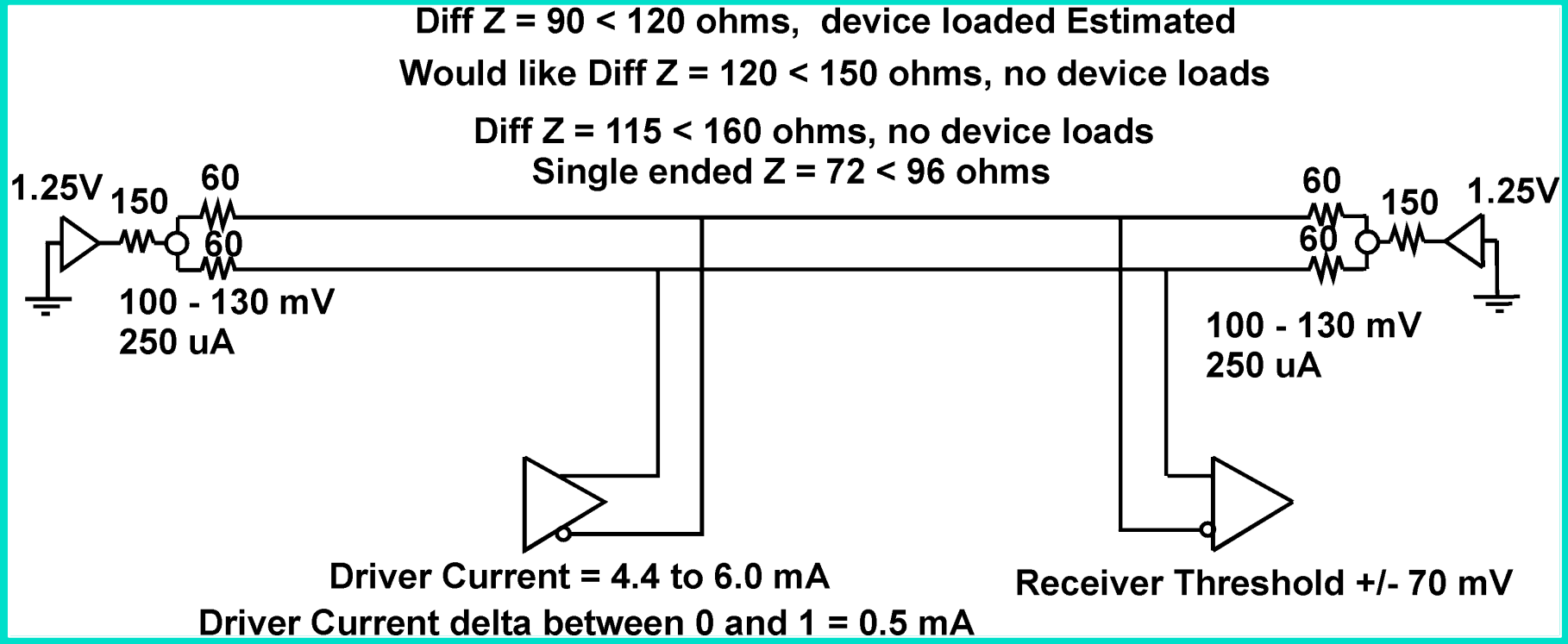
SPI-2 LVDS Termination



SPI-2 LVDS Diff Sense



SPI-2 LVDS Bus



June 21, 1995 Merrimack MTG

- Reviewed the document sections of SPI that will be effected by LVDF SPI.
- Studied the Diff Sense issues and set new values
- Reviewed common mode issues with each interface
- Reviewed the cost objectives of LVDS
- Defined the pinning for the based on Single ended, regenerated table done in Harrisburg, but not documented.
- Note: FAST-40 single ended would still be a longer distance than ATA. This should be a viable standard.
- FAST-40 and FAST-80 will require very low delta stub and capacitance for data, parity, ack and req signals. The additive effect of 7 or 15 devices will exceed the skew budget.
- Worked timing issues for FAST-40 and FAST-80, external drivers and receivers can not be used, there is no margin in the skew budget.

Agreements Sept 95

- A single chip may work for both single ended (Async, 5, 10, 20) or LVDS (FAST-40, 80)
- No SE FAST-40 - Objection, Seagate, QLogic - Package Pin count issue
- No SE Signals in FAST-40+ LVDS - Objection Quantum
- Current Timing Diagram OK
- Diff sense is define with an autosense feature.
- low, (SE mode) all ground drivers shall be ON all the time.
- Pin outs OK
- Target of 15 pF maximum
- 4 < 6 mA Current mode Driver, no Driver output impedance spec.
- Terminator bias with current limited, 150 mV at 250 microAmps maximum.
- No specified receiver hysteresis.

Agreements Oct 13,1995

- Driver lower current limit was increase to 4.4 mA.
- Receiver thresholds must be reduced to +/-70 mV.
- Terminator bias was reduced to 100-130 mV.
- Termination should be discribed as the current/voltage function. Too much specific implementation information.
- Crosstalk from single-ended to LVDS is too high to allow a hybrid system, if Common mode were not enough.

LVDS Power Calculations

- Original calculations
- Transceiver power calculations for a 27 line device at 3.3 Volts + 10%.
- Maximum 21 Active Drivers on a 27 line device.
- 27 Active Receivers
- Driver control current 1 mA * 3.6 Volts, 3.6 mW * 21 Lines = 75.6 mW
- Driver power 4 mA * (3.6-.24) Volts, 13.6 mW * 21 Lines = 285.6 mW
- Receiver Power 2.5 mA * 3.6 Volts, 9 mW * 27 Lines = 243 mW
- Total Transceiver current 604.2 mW

LVDS - 6 mA Power

- Transceiver power calculations for a 27 line device at 3.3 Volts + 10%.
- Maximum 23 Active Drivers on a 27 line device.
- 6 Active Receivers
- Driver control current 1 mA * 3.6 Volts, 3.6 mW * 23 Lines = 82.8 mW
- Driver power 6 mA * (3.6-.36) Volts, 19.44 mW * 23 Lines = 447.12 mW
- Receiver Power 2.5 mA * 3.6 Volts, 9 mW * 4 Lines = 36 mW
- Total Transceiver current 565.92 mW
- Updated 9-Nov-95