SCSI SPI-2 Low Voltage Differential Signaling

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1.0 Introduction:

The Low Voltage Differential Signaling (LVDS) specification, SP-3357 which will become EIA/TIA 644, is specified like EIA422 for a single driver with multiple receivers and the single driver is at one end of the bus. The SCSI Low Voltage differential standard will have to be like EIA485 where the driver and receiver can be any where on the bus. The driver power however must remain low. The Low Voltage differential is based on a current drive. The output current of the drivers must remain low, this requires adjusting the specification for termination on both ends of the bus with a differential characteristic impedance of 120 ohms and leaving a common mode impedance with a bias. The changes from the Low Voltage Differential standard will be in the voltages measured, the drive current will remain the similar to the SP-3357 specification. This will allow the drivers to be integrated into the controller maintaining the cost of low voltage differential in line with the single ended SPI implementations.

The receiver thresholds must be adjusted down from the SP-3357 specification to compensate for the lower drive voltage because of the termination on both ends of the line.

This is a second pass at adjusting the SP-3357 standard to the SCSI SPI-2 requirements. The basic 655 MBPS serial parameters appear to meet the longer term SPI goals of well over 100 megatransfer rates allowing for long term migration strategy for parallel SCSI. The initial version of the standard is being written for FAST-40 and FAST-80, future versions could include FAST-160 and FAST-320, over 320 megatransfer rates Skews may not be manageable. This should carry SPI through the year 2000, after 2000 FPI migration would be the logical strategy when the industry requires over 640 megabytes per second parallel fiber optics will most likely be the best migration path.

The high speed standard requires several new physical limitations, as the speed increases the skews become much more important. It is important to design the new standard for future migration increasing the speed. This requires line to line matching of drivers, receivers, capacitance and stub lengths to minimize the skew. Delta are more important than the physical delay time. The delta stub and capacitance difference between lines is most important on the devices, where there can be up to 15 devices of the same design on a single bus.

It is the intent that controllers will be built that can drive both low voltage differential and single ended depending on the bus configuration for the first generation. If all of the devices are low voltage differential then the system will run on low voltage differential, but if one or more devices or any system component is single ended then all the devices revert back to single ended. This will allow backward compatibility with the forward migration path for the first generation of low voltage differential. This document only deals with low voltage differential electrical levels and how to determine if the type of bus the device is attached to.

The devices for FAST-80 and higher may only be LVDS, not supporting the single ended devices.

The distance goal is 12 meters for FAST-40 & FAST-80. Testing will have to be done to insure adequate margin for 12 meters with 7 to 15 different bus loads.

2.0 Basic Driver Concepts and Requirements

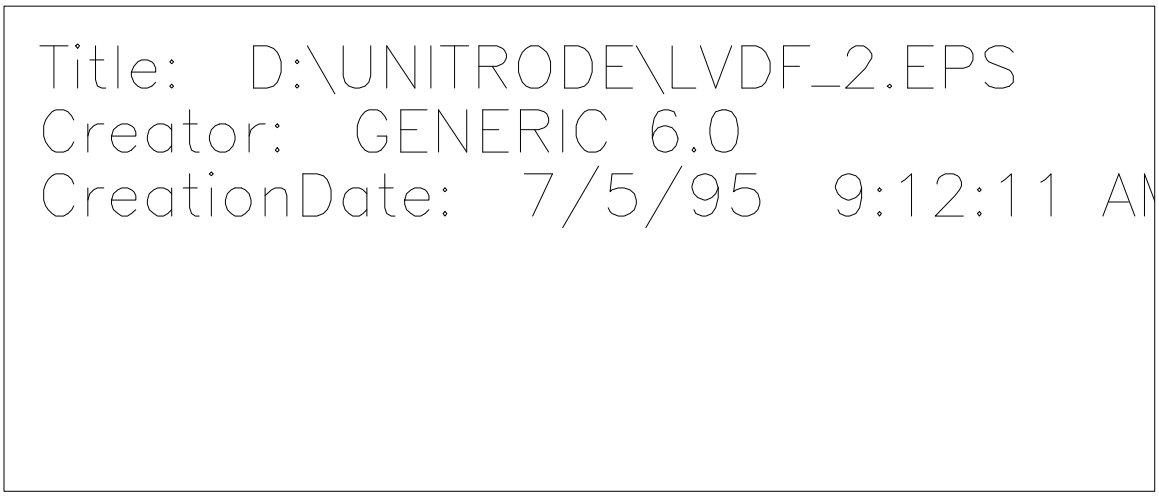
The low voltage differential driver is required to have a high degree of balance to minimize distortion and radiation. The driver is current based with a drive current range of 4.4 to 6.0 mA into a 60 ohm load with a common mode termination of 75 ohms to 1.25 Volts. This will produce a static signal of 264 to 360 mV with a common mode voltage of 1.25 volts. The low common mode will allow migration to lower voltage logic families, 3.3 Volts and 2.5 Volts.

The drivers shall drive the bus to the failsafe state for one round trip time of the bus before tristating. Note: The terminators only provide a low current bias, the time to pull the bus to the failsafe state with the terminators would be too long with the terminator current restrictions. One round trip time for 12 meters would be 120 ns. The terminators only hold the line with a low bias current to the bias (failsafe) state.

2.1 Driver Characteristics

The driver output voltage is measured with two 30 ohm resistors in series load and a 75 ohm common mode termination to 1.25 Volts, the differential output voltage shall be 264 to 360 mV. The Output state will match the normal communications standards with the VA-VB voltage of -264 to -360 mV for a 1 state and +264 to +360 mV for a 0 State, with a maximum delta of 30 mV. The common mode voltage shall be 1.125 to 1.275 Volts with a maximum delta of 30 mV.

The driver open circuit output voltage VA-VB open circuit voltage may be close to the supply voltages. The standard does not restrict the voltage other than it shall be less than the supply voltages, 3.6 Volts Maximum.



2.2 Driver Short Circuit Measurements

Shorting the driver to ground the output current shall not exceed 24 mA in either state.

Shorting the differential driver output the current shall not exceed 12 mA in either state.

2.3 Driver Tristate Line Load Test

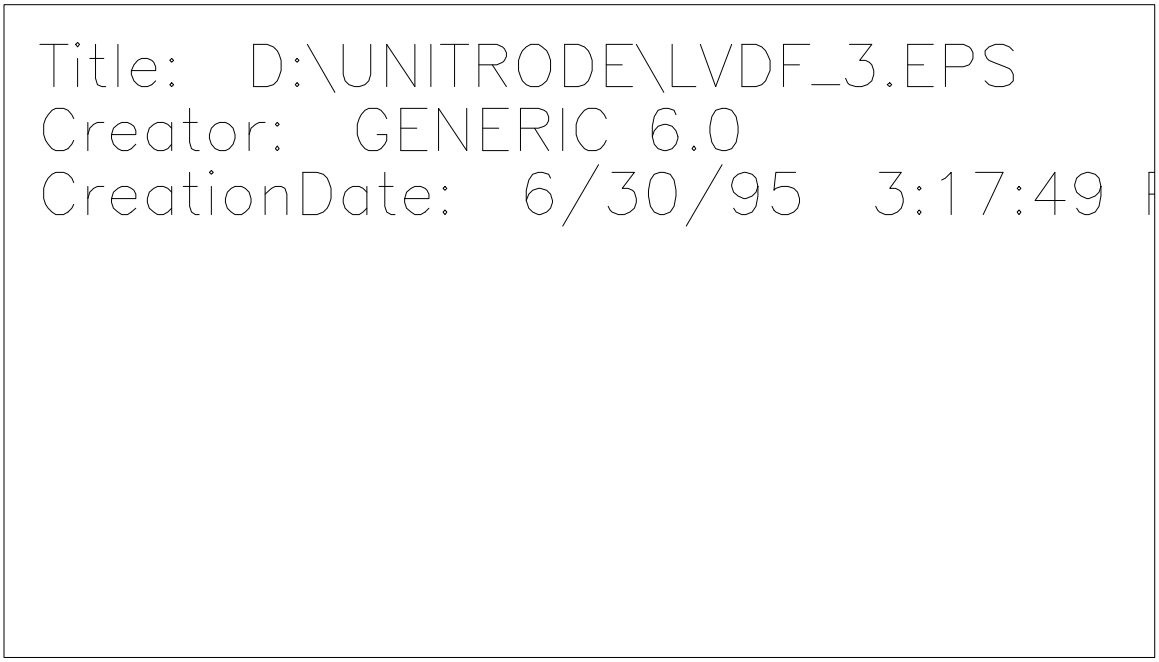
The SCSI SPI-2 applications combines the driver and receiver, the load for the driver and receiver combination see the receiver section 3.1

2.4 Driver Output Signal Waveform and Balance
The output signal wave form shall be measured with two 30 ohm resistors in series with a 5 pF differential Cl.

The rise and fall time is measured at the 20 and 80% points of the steady state voltage, Vss. The rise and fall time shall be 0.5 to 1.5 ns. (Note this fixes the rise and fall time to allow maximum future migration by only adjusting the timing.)

The overshoot and ringing shall be less than 20% of Vss.

The common mode dynamic imbalance, delta VOS shall be less than 100 mV.



3.0 Receiver Characteristics

The receiver shall operate over a common mode range of +0.05 to 2.35 Volts with a running speed maximum differential threshold of +/-70 mV. The maximum differential receiver input voltage may be as high as the 3.6 Volt supplies. The maximum receiver input voltage with respect to ground shall not be greater than 2.4 volts or less than ground. The receiver input impedance shall be high reducing the loading effects.

3.1 Transceiver load characteristics

The transceiver input current shall be less than 10 μA from 0 to 2.4 Volts when the other I/O pin is held at 1.2 Volts +/- 50 mV. Total device capacitance including etch and connectors shall be less than 15 pF, measured in single ended mode, as specified in SPI.

3.2 Receiver Failsafing

ACK, REQ, BSY and RESET receiver failsafing is recommended for Open or Shorted cable, and a bus without termination/termpwr applied. The receiver may detect a bus failsafe state when the voltage remains below 50 mV levels for an extended period of time. The suggested time is 1 μs for the extended time period.

4.0 Termination

There shall only be two terminators enabled, one at each end of the bus.

The termination shall provide the differential and common mode termination with failsafe biasing. The termination shall be low power with a low idle current of less than 30 mA for 27 differential lines, a resistor divider network is not allowed.

The differential termination shall be 120 ohms +/-5 % with a bias voltage of 100 to 130 mV, low current 220 to 250 μA in the failsafe state. The line Asserted state the bias generator acts like an ideal forward bias diode and must handle at least 35 mA. The line negated state the bias generator acts line a zener diode, when more than 150 mV signal is applied it limits the voltage across the bias generator with a minimum of 4 mA current capability. The current must be limited to not effect the signal integrity with the low current drivers. Electrically when the bus is driven the termination looks like 120 Ohms differential and 150 ohms to 1.25 Volts.

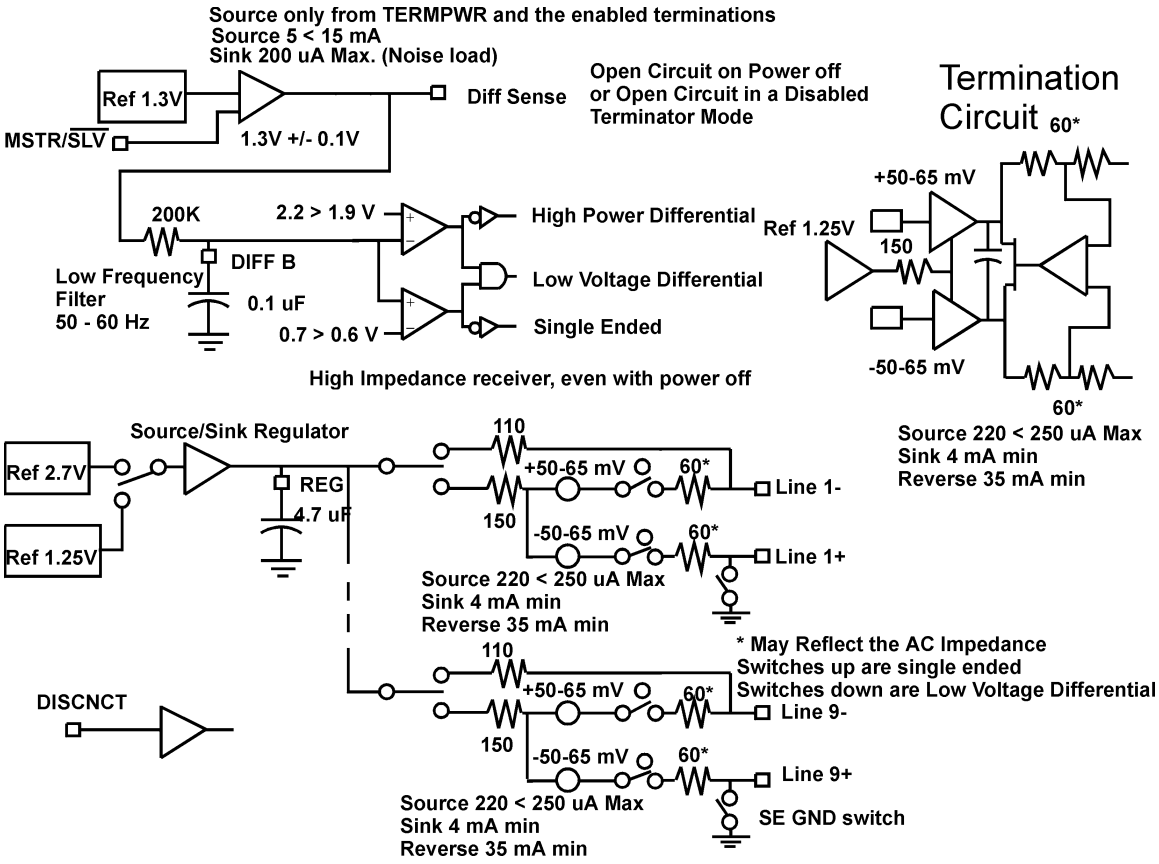
The ideal zener is built using a FET clamp circuit for the forward bias. When the terminator detects the line driven in the reverse direction it clamps the bias generators with the FET, the FET will handle the full 35 mA possible for SCAM arbirtation when it is possible to have all the drivers turned on. The bias generators are light source, heavy sink. The light source bias the line with 220 to 250 uA of current, but when the line is driven it becomes a heavy sink, 4 mA plus more than the maximum drive current..

The 40 - 80 pF capacitor across the bias generator/clamp is to respond to the high speed switching of the line, the clamp and bias generators need about 5 ns to respond to the line transients.

The common mode termination shall be 150 ohms +/-10% with a bias voltage of 1.25 Volts +/- 50 mV.

Note: A resistor divider network like the one used in high power differential SCSI would force an overall bias to the signal when the low current drive signals of LVDS are used. This would reduce the signal length that could be achieved by LVDS and would be a constant load on the TERMPWR line.

It is the intent for SCSI LVDS to be as low of power as possible and and robust as possible. This will give the user the best cost performance standard for disk connection. This makes the terminator more complex but improves the system margin and reduces the terminator power, which is a constant. Battery systems can not afford a high terminator idle current.


Source only from TERMPWR and the enabled terminations
Source 5 < 15 mA
Sink 200 uA Max. (Noise load)
Ref 1.3V
MSTR/SLV
1.3V +/- 0.1V
Diff Sense
Open Circuit on Power off
or Open Circuit in a Disabled
Terminator Mode
Termination
Circuit 60*
200K
2.2 > 1.9 V
High Power Differential
DIFF B
Low Frequency
Filter
50 - 60 Hz
0.1 uF
Low Voltage Differential
0.7 > 0.6 V
Single Ended
High Impedance receiver, even with power off
+50-65 mV
Ref 1.25V
150
-50-65 mV
60*
Source 220 < 250 uA Max
Sink 4 mA min
Reverse 35 mA min
Source/Sink Regulator
Ref 2.7V
Ref 1.25V
REG
4.7 uF
110
+50-65 mV
60*
Line 1-
150
-50-65 mV
Line 1+
Source 220 < 250 uA Max
Sink 4 mA min
Reverse 35 mA min
* May Reflect the AC Impedance
Switches up are single ended
Switches down are Low Voltage Differential
DISCNCT
Line 9-
Line 9+
SE GND switch
Source 220 < 250 uA Max
Sink 4 mA min
Reverse 35 mA min

4.1 Diff Sense

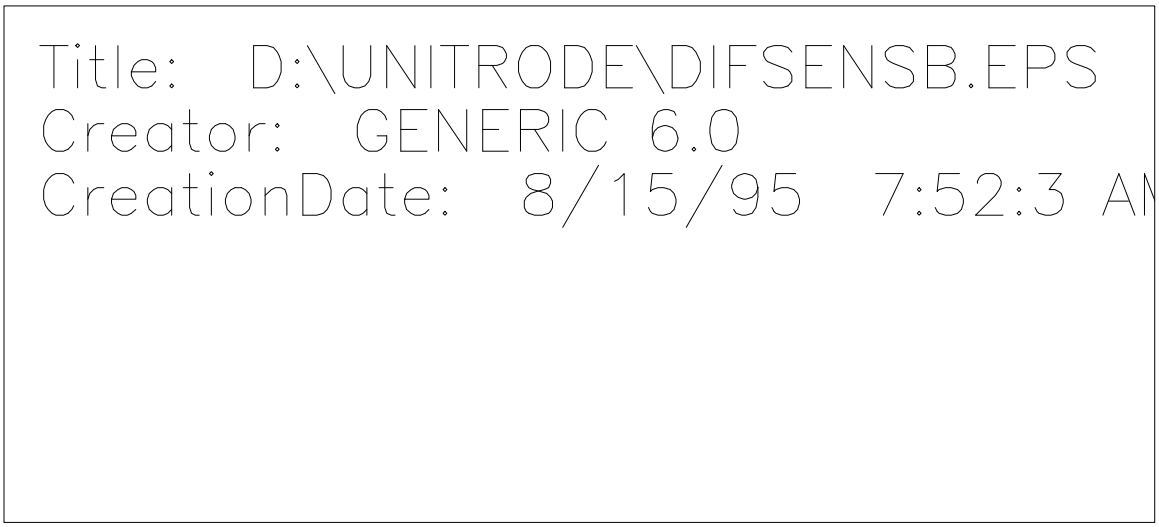
Only the enabled terminators at the end of the bus shall provide a bias current to the differential sense line 1.3 Volts +/-0.1V sourcing 5 to 15 mA, Sinking 200 µA Max.

Circuits for the diff sense detection shall filter out noise with a 20K ohm series resistor and a 0.1 µF capacitor. Below 0.6 volts shall be detected as single ended, 0.7 to 1.9 Volts shall be detected as low voltage differential, above 2.2 Volts shall be detected has EIA485 standard differential SCSI.

A 200K ohm pulldown resistor on the input of Diff Sense for open circuit condition.

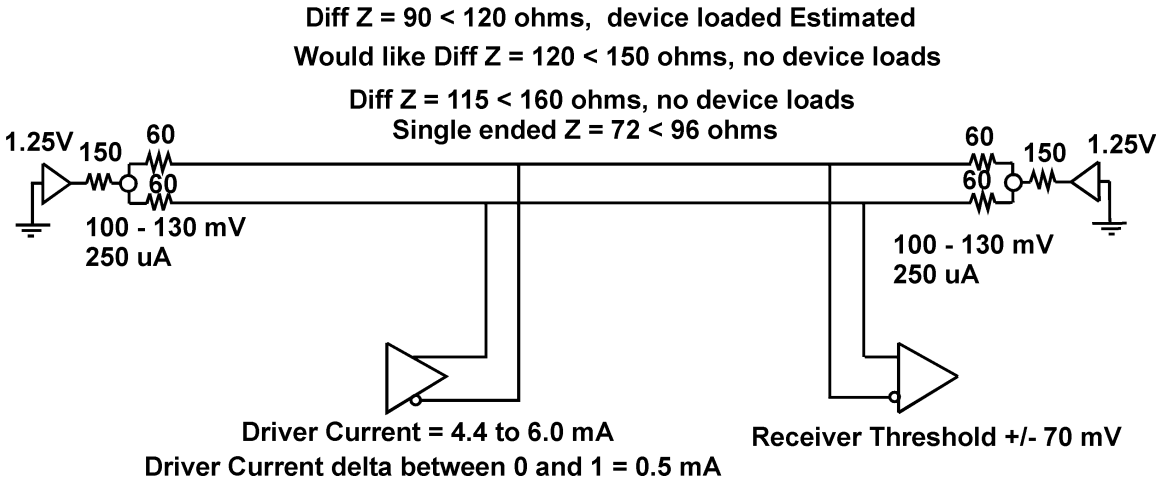
When the terminator detects single ended, and has the capability to terminate the single ended line. The Positive line will be connected driven to ground and the negative line will revert to the standard single ended termination as defined in FAST-20.

When the terminator detects High power - EIA485 type devices it will shut down. High powered differential uses a different pinout, and can have very high common mode voltages. (May need to be reviewed for a better option ?)



5.0 Bus view of the System

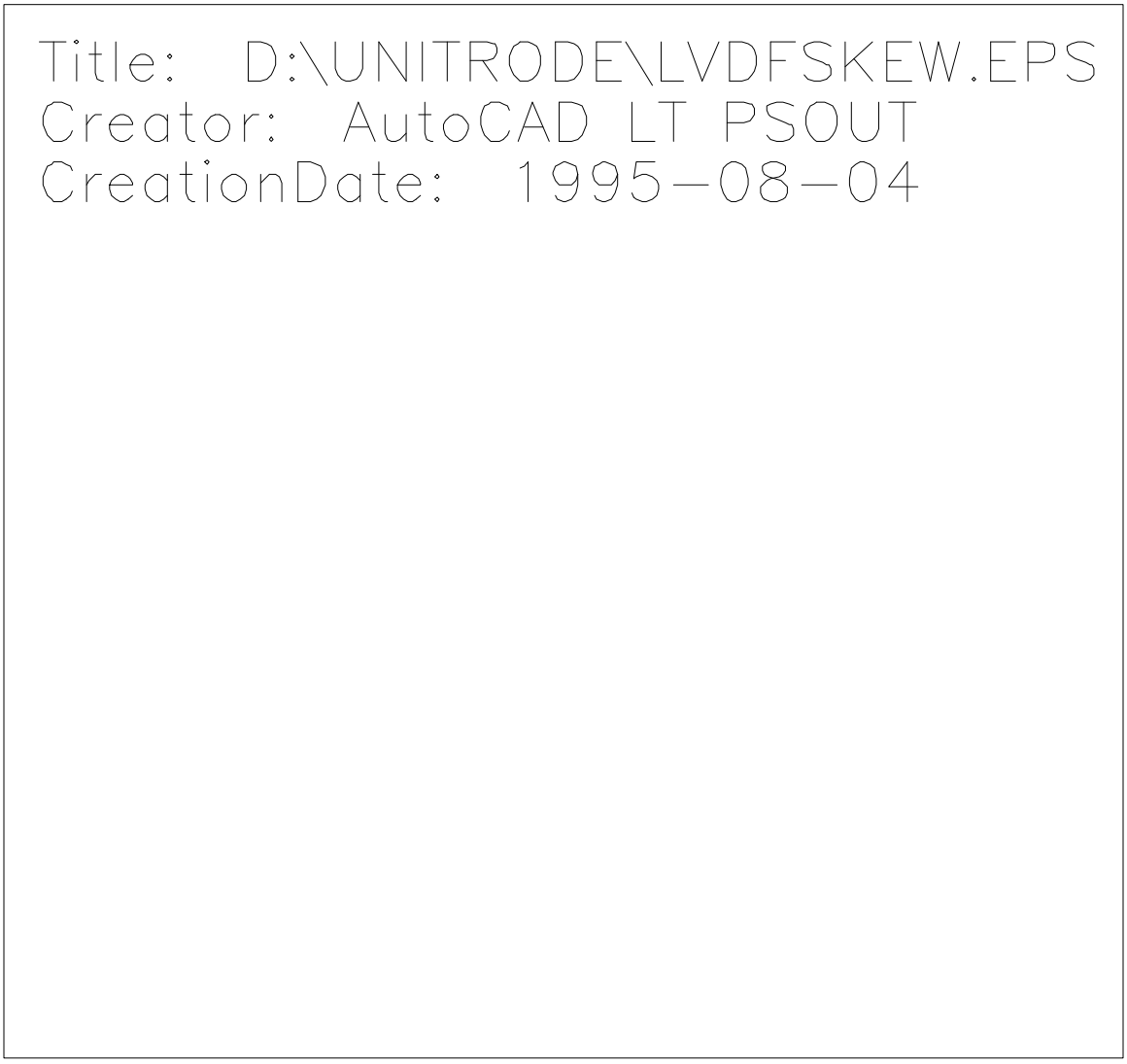
The overall system allows for a DC common mode voltage of +/- 0.6 Volts, but allows an AC common mode of +/- 1.2 Volts above 40 Hz. The receivers and drivers will allow for 0 to 2.4 Volts maximum voltage range in reference to ground.



5.1 System SKEW Issues

The higher speed operation requires skew to be reduce on the devices and controllers. The skew for devices can add up when up to 15 devices of the same type are used on the sample bus, each device will delta skew will add. The delta etch and package length of signal lines on a device or target shall be less than 0.5 inches. The delta capacitance shall be less than 5 pF.

The delta skew within a differential pair shall be less the 25 ps.



6.0 Power Budget

A key goal is to design a interface that transceivers can be incorporated into the controller chip, to do this the power must be limited in the transceivers to about 500 mWatts. The transceivers incorporated in the controller drastically effect the skew budget, allowing for much higher speed operation.

The power table was developed in the July & August meetings.

- **Transceiver power calculations for a 27 line device at 3.3 Volts + 10%.**
- **Maximum 21 Active Drivers on a 27 line device.**
- **6 Active Receivers**
- **Driver control current 1 mA * 3.6 Volts, 3.6 mW * 21 Lines = 75.6 mW**
- **Driver power 6 mA * (3.6-.36) Volts, 19.44 mW * 21 Lines = 408.24 mW**
- **Receiver Power 2.5 mA * 3.6 Volts, 9 mW * 6 Lines = 54 mW**

Total Transceiver current 537.84 mW