SCSI SPI-2 Low Voltage Differential

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1.0 Introduction:

The Low Voltage differential specification is specified like EIA422 for a single driver with multiple receivers and the single driver is at one end of the bus. The SCSI Low Voltage differential standard will have to be like EIA485 where the driver and receiver can be any where on the bus. The driver power however must remain low. The Low Voltage differential is based on a current drive. The output current of the drivers must remain low, this requires adjusting the specification for termination on both ends of the bus with a differential characteristic impedance of 120 ohms and leaving a common mode impedance with a bias. The changes from the Low Voltage Differential standard will be in the voltages measured, the drive current will remain the similar to the SP-3357 specification. This will allow the drivers to be integrated into the controller maintaining the cost of low voltage differential in line with the single ended SPI implementations.

The receiver thresholds must be adjusted down to compensate for the lower drive voltage because of the termination on both ends of the line.

This is a first pass at adjusting the SP-3357 standard to the SCSI SPI-2 requirements. The basic 655 MBPS serial parameters appear to meet the longer term SPI goals of well over 100 megatransfer rates allowing for long term migration strategy for parallel SCSI.

The high speed standard requires several new physical limitations, as the speed increases the skews become much more important. It is important to design the new standard for future migration increasing the speed. This requires line to line matching of drivers, receivers, capacitance and stub lengths to minimize the skew. Delta are more important than the physical delay time.

It is the intent that controllers will be built that can drive both low voltage differential and single ended depending on the bus configuration. If all of the devices are low voltage differential then the system will run on low voltage differential, but if one device will not then all the devices revert back to single ended. This will allow backward compatibility with the forward migration path. This document only deals with low voltage differential electrical levels and how to determine if the type of bus the device is attached to.

2.0 Basic Driver Concepts and Requirements

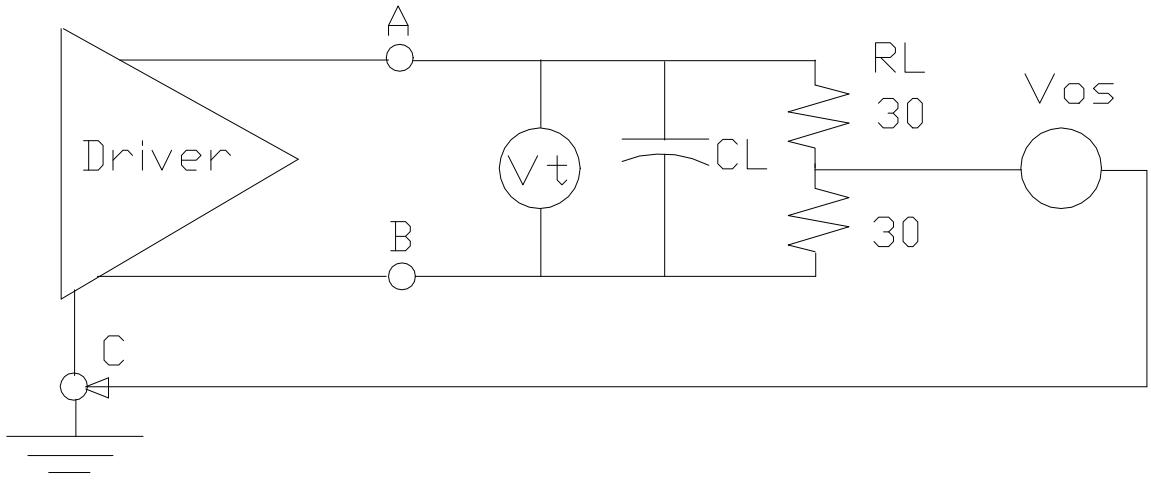
The low voltage differential driver is required to have a high degree of balance to minimize distortion and radiation. The driver is current based with a drive current range of 3.0 to 4.0 mA into a 60 ohm load. This will produce a static signal of 180 to 240 mV with a common mode voltage of 1.25 volts. The low common mode will allow migration to lower voltage logic families, 3.3 Volts and 2.5 Volts.

The drivers shall drive the bus to the failsafe state for one round trip time of the bus before tristating. Note: The terminators only provide a low current bias, the time to pull the bus to the failsafe state with the terminators would be too long with the terminator current restrictions.

2.1 Driver Characteristics

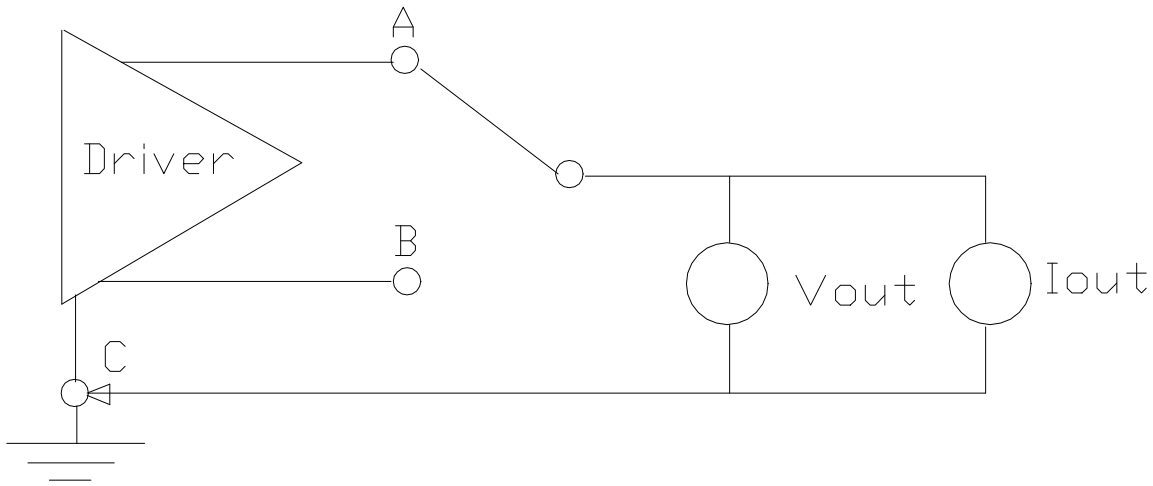
The driver output voltage is measured with two 30 ohm resistors in series load, the differential output voltage shall be 180 to 240 mV. The Output state will match the normal communications standards with the VA-VB voltage of -180 to -240 mV for a 1 state and +180 to +240 mV for a 0 State, with a maximum delta of 30 mV. The common mode voltage shall be 1.125 to 1.275 Volts with a maximum delta of 30 mV.

The driver open circuit output voltage VA-VB shall not exceed 500 mV.



2.2 Driver Output Impedance

The driver output impedance shall be in the range of 40 to 140 ohms and shall be within 10% whether in the high or the low state.



2.3 Driver Short Circuit Measurements

Shorting the driver to ground the output current shall not exceed 24 mA in either state.

Shorting the differential driver output the current shall not exceed 12 mA in either state.

2.4 Driver Tristate Line Load Test

The SCSI SPI-2 applications combines the driver and receiver, the load for the driver and receiver combination see the receiver section 3.x

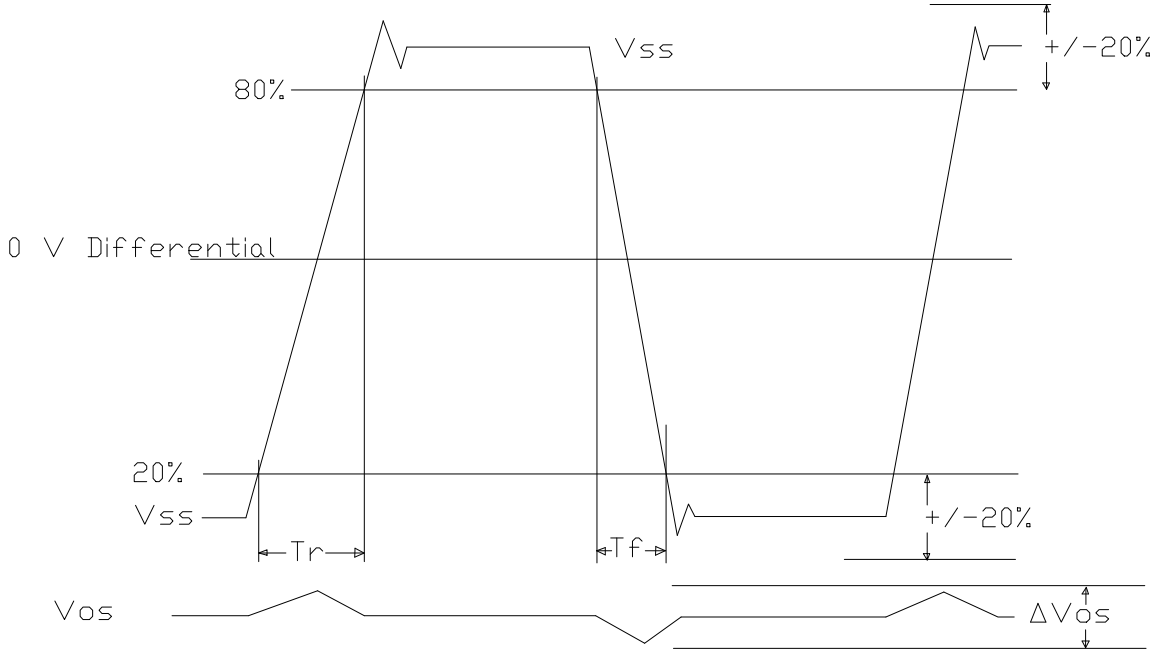
2.5 Driver Output Signal Waveform and Balance

The output signal wave form shall be measured with two 30 ohm resistors in series with a 5 pF differential Cl.

The rise and fall time is measured at the 20 and 80% points of the steady state voltage, Vss. The rise and fall time shall be 0.5 to 1.5 ns. (Note this fixes the rise and fall time to allow maximum future migration by only adjusting the timing.)

The overshoot and ringing shall be less than 20% of Vss.

The common mode dynamic imbalance, delta VOS shall be less than 100 mV.



3.0 Receiver Characteristics

The receiver shall operate over a common mode range of +0.05 to 2.35 Volts with a maximum differential threshold of +/-50 mV. The maximum differential receiver input voltage shall be less than 550 mV. The maximum receiver input voltage with respect to ground shall not be greater than 2.4 volts or less than ground. The receiver input impedance shall be high reducing the loading effects.

3.1 Transceiver load characteristics

The transceiver input current shall be less than 20 μA from 0 to 2.4 Volts when the other I/O pin is held at 1.2 Volts +/- 50 mV.

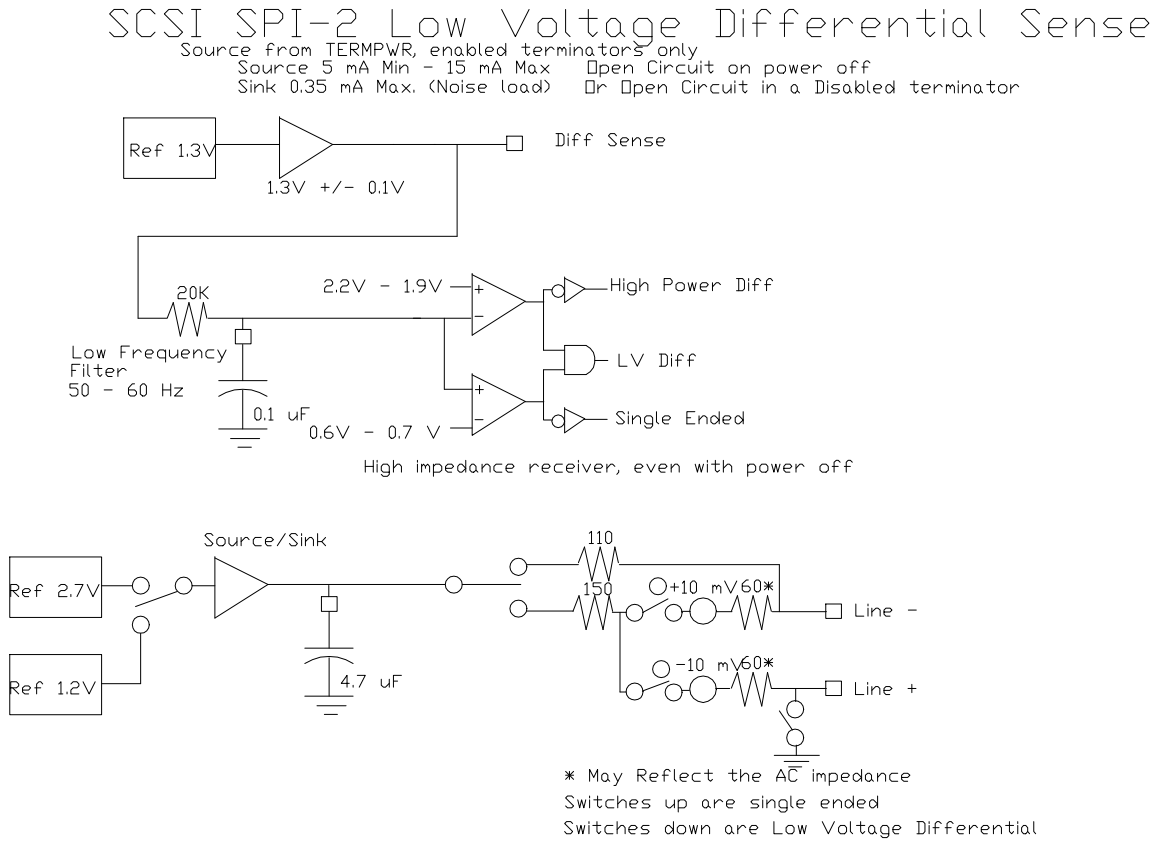
4.0 Termination

There shall only be two terminators enabled, one at each end of the bus.

The termination shall provide the differential and common mode termination with failsafe biasing. The termination shall be low power with a low idle current, a resistor divider network is not allowed.

The differential termination shall be 120 ohms +/-10 % with a failsafe bias voltage of 20 to 40 mV, low current 0.15 mA maximum. The current must be limited to not effect the signal integrity with the low current drivers.

The common mode termination shall be 150 ohms +/-10% with a bias voltage of 1.25 volts +/- 50 mV.



4.1 Diff Sense

Only the enabled terminators at the end of the bus shall provide a bias current to the differential sense line 1.3 Volts +/-0.1V sourcing 5 to 15 mA, Sinking 0.35 mA Max.

Circuits for the diff sense detection shall filter out noise with a 20K ohm series resistor and a 0.1 µF capacitor. Below 0.6 volts shall be detected as single ended, 0.7 to 1.9 Volts shall be detected as low voltage differential, above 2.2 Volts shall be detected has EIA485 standard differential SCSI.

A 100K ohm pulldown resistor on the input of Diff Sense for open circuit condition.