SPI-2 FRAMEWORK

THE ELEMENTS OF SPI-2 ARE TAKING SHAPE:

- **A BASIC INTERFACE ARCHITECTURE IS PROPOSED**
  - **SUPPORTS BOTH SE AND DF IN THE SAME SILICON**
  - **USES THE SAME CONNECTORS AND CABLES AS SPI/FAST 20**
  - **AUTODETECTS TRANSMISSION SCHEME BEING USED AND SETS TRANSCEIVERS ACCORDINGLY**
  - **REQUIRES FULL DF PATH EVERYWHERE FOR DF BUT IS COMPATIBLE WITH A SE ONLY (COMMONED GROUNDS ETC) OR DF PATH (BOTH + AND - SIGNALS) FOR SE**
  - **HAS BETTER REAL COMMON MODE PERFORMANCE THAN TODAY'S DF**
  - **REPINS THE DF TO BE FUNCTIONALLY COMPATIBLE WITH SE**

SPI-2 FRAMEWORK

THE ELEMENTS OF SPI-2 ARE TAKING SHAPE:

- **A TIMING BUDGET FOR FAST 40 AND FAST 80 IS PROPOSED**
  - **BUILDS OFF THE PRESENT FAST 20 DF RECEIVER TIMINGS**
  - **PRESERVES ALL THE FAST 20 PULSE DISTORTION SKEW**
  - **RECLAIMS HALF OF THE "FAT" IN THE PRESENT CABLE SKEW (SAME CABLES)**
  - **GAINS MUCH FROM THE ELIMINATION OF SEPARATE TRANSCEIVERS**

- **THE VHDCI CONNECTION SCHEME IS STABILIZING FOR CABLED CONNECTIONS**

- **THE SCA-2 DEVICE CONNECTOR IS STABILIZING**

- **NEW UNIVERSAL AUTOSENSE TERMINATORS ARE PROPOSED**

SPI-2 FRAMEWORK

THE ELEMENTS OF SPI-2 ARE TAKING SHAPE:

- COST IMPACTS OF “EXTRA” PINS HAVE BEEN ADDRESSED

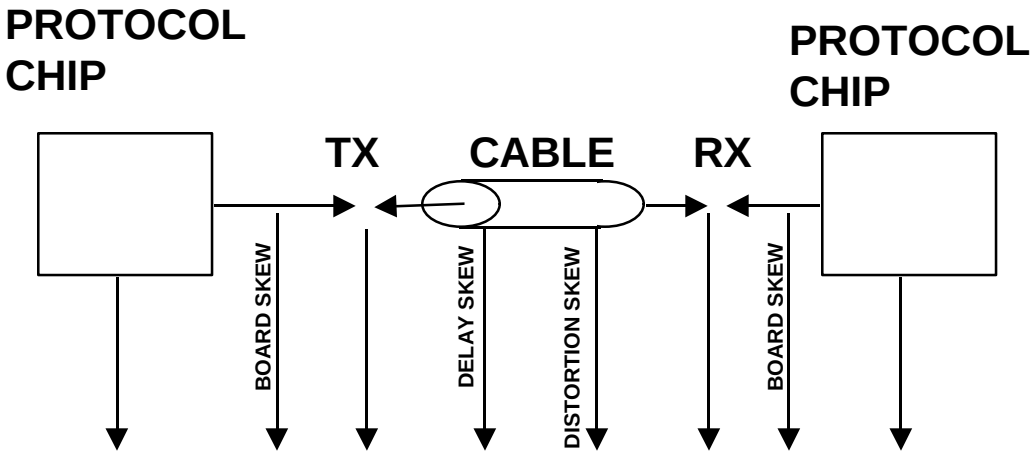
- THE MAJOR IMPACTS OF 3.3 VOLT SUPPLIES HAVE BEEN ADDRESSED:
  - DROPOUT VOLTAGES FOR SE TERMINATORS
  - EFFECTS OF TERMPWR DISTRIBUTION
  - CHIP INPUT LEVELS

- COMPLETE DIFFSENS STRATEGY IS PROPOSED (INCLUDING LOW FREQUENCY GROUND SHIFT)

- HIGH FREQUENCY COMMON MODE ACTUALLY BETTER THAN WITH HIGH POWER DIFFERENTIAL

SPI-2 FRAMEWORK

SETUP AND HOLD TIMINGS



FAST									
10 SE	24	1.0	23	4.0	4.0	15	1.0	14	SETUP
	34		33			25		24	HOLD
20 SE	12	0.5	11.5	3.0	2.0	6.5	0.5	6	
	17		16.5			11.5		11	
10 DF	32	9*	23	4.0	4.0	15	10*	5	
	42		33			25		15	
20 DF	16	4.5*	11.5	3.0	2.0	6.5	5.5*	1	
	21		16.5			11.5		6	
40 SE/DF	5	0.25	4.75	1.5	2.0	1.25	0.25	1	
	9		8.75			5.25		5	
80 SE/DF	5	0.25	4.75	1.5	2.0	1.25	0.25	1	
	6.5		6.25			2.75		2.5	

*** INCLUDES SEPARATE TRANSCEIVER SKEW**

SPI-2 FRAMEWORK

COST IMPACT OF "EXTRA PINS"

- **WIDE DIFFERENTIAL REQUIRES MORE PINS THAN SINGLE ENDED (APPROX 20 - NOT 27 - MORE) -- ALL SIGNALS, EVEN "LOW SPEED" CONTROL SIGNALS NEED TO BE DIFFERENTIAL**

- **FAST 40/80 REQUIRES DIFFERENTIAL**

- **A UNIVERSAL SCSI INTERFACE MUST SUPPORT DIFFERENTIAL**

- **THEREFORE THE UNIVERSAL SOLUTION IMPOSES A COST PREMIUM FOR SINGLE ENDED ONLY APPLICATIONS DUE TO THE PIN COUNT INCREASE**

- **THIS COST NEEDS TO BE UNDERSTOOD AND WEIGHED AGAINST THE BENEFITS OF NOT NEEDING MULTIPLE SCSI INTERFACES**

- **ESTIMATES OF THE CHIP PACKAGING ARE:**

  160 SE VS 180 DF PINS FOR 32 BIT PCI HOST CHIPS
  144 SE VS 164 DF PINS FOR TARGET CHIPS
  ~208 SE VS 230 DF PINS FOR 64 BIT PCI HOST CHIPS

  THIS DRIVES ~$1 TO 3 INCREASE / INTERFACE FOR THE UNIVERSAL SOLUTION

SPI-2 FRAMEWORK

KEY QUESTION:

HOW SHOULD WE ADDRESS THE INCREASING PROTOCOL OVERHEAD AS THE DATA PHASE SPEED INCREASES??

HOW MUCH OF THIS OVERHEAD IS PROTOCOL LIMITED AND HOW MUCH IS IMPLEMENTATION INEFFECIENCY??

CAN WE GAIN MAJOR OVERHEAD REDUCTIONS BY REDUCING THE OVERALL PROPAGATION DELAY RELATED PARAMETERS (IN EFFECT BY REDUCING THE BUS LENGTH)??

DO WE NEED A NEW MESSAGING SYSTEM??

SHOULD THIS BE A SPI-2 ISSUE??