Quantum

Date: June 21, 1995
To: ATA Committee
From: Jim McGrath (408-8944504)
Subject: Comments on WD proposal

Feedback on various provisions:

1) Would like to postpone the entire topic of interleaved DMA. Specifically, no byte count value returned by drive. It is unclear whether that byte count is handled in 1 burst DMA, 1 release sequence,...

2) SERVICE command (A2) - do we need to write to the command register, or is another handshake OK (e.g. write to another take file register). Command register breaks existing hardware.

3) If we keep the DMA bit (see below), make it bit 7 not bit 0 of the tag/DMA register.

4) On the take file register contents for read/write overlap/queuing commands, the tag/DMA bit should be in the sector count register, with the sector count in the features register. This allows the CHS to be returned on errors for information (queue is still cleared on an error).

5) Have an error bit to report queue cleared on an error.

   Require that if a non tagged command is being executed, an overlap/queued command will abort both commands.

6) Assert DREQ before releasing BSY on the receipt of a command to allow the first read/write transfer of an overlapped/queueed command to be done without an interrupt.

7) On read/write overlap queued, we should use 4 op codes for read/write and P10/DMA, not have direction encoded in op code and type of transfer in a register bit.