Accredited Standards Committee
X3, Information Technology

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Reply to: John Lohmeyer

To: Membership of X3T10

From: Ralph Weber, Secretary X3T10
John Lohmeyer, Chair X3T10

Subject: Minutes of SPI Futures Study Group Meeting
Harrisburg, PA -- May 8, 1995

Agenda

1. Opening Remarks

2. Approval of Agenda

3. Attendance and Membership

4. Physical Topics
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Results of Meeting

1. Opening Remarks

John Lohmeyer, the X3T10 Chair, called the meeting to order at 9:00 a.m., Monday May 8, 1995. He thanked Chuck Brill of AMP, Inc. for arranging and hosting the meeting. The meeting was held at the Sheraton Inn, in Harrisburg, PA.

As is customary, all those present introduced themselves and a copy of the attendance list was circulated. John noted that the meeting is an ad hoc meeting of the X3T10 committee. John reminded everyone of the X3T10 rules and noted that votes taken at this meeting (if any) have no binding effect on X3T10.

2. Approval of Agenda

The agenda was approved.

3. Attendance and Membership

Attendance at study group meetings does not count toward minimum attendance requirements for X3T10 membership. Study group meetings are open to any person or organization directly and materially affected by X3T10's scope of work.

The following people attended the meeting:

Name	S	Organization	Electronic Mail Address
Mr. Norm Harris	P	Adaptec, Inc.	nharris@eng.adaptec.com
Mr. Lawrence J. Lamers	A#	Adaptec, Inc.	ljlamers@aol.com
Mr. Charles Brill	P	AMP, Inc.	cebrill@amp.com
Mr. Bob Whiteman	A	AMP, Inc.	whiteman@cup.portal.com
Mr. Bob Atkinson	V	AMP, Inc.	rdatkins@amp.com
Mr. Louis Grantham	P	Dallas Semiconductor	grantham@dalsemi.com
Dr. William Ham	A#	Digital Equipment Corp.	ham@subsys.enet.dec.com
Mr. Ralph O. Weber	A#	ENDL Associate	roweber@acm.org
Mr. Duncan Penman	P	IIX Consulting	penman@netcom.com
Mr. Dean Wallace	P	Linfinity Micro	
Mr. Chuck Grant	A	Madison Cable Corp.	charles_grant@madisonusa.ccmail.compuserve.com
Mr. Skip Jones	P	QLogic Corp.	sk_jones@qlc.com
Mr. John Lohmeyer	P	Symbios Logic Inc.	john.lohmeyer@symbios.com
Mr. Tracy Spitler	V	Symbios Logic Inc.	tracy.spitler@symbios.com
Mr. Paul D. Aloisi	P	Unitrode Integrated Circuits	Aloisi@uicc.com

15 People Present

Status Key:
- P - Principal
- A,A# - Alternate
- O - Observer
- L - Liaison
- V - Visitor

4. Physical Topics

4.1 Overview of Current Status [Ham]

Bill Ham reported on both historical activities and very recent work in parallel SCSI futures.

SUMMARY OF SPI FUTURES -- MAY 8, 1995

Recent work by the SPI Futures Study Group has defined future directions in five key areas. This document describes each of these areas and gives comments on the present status.

The five areas are:

1) Server SPI (Higher speed, simplified common single ended/differential interface)
2) Physical System Interconnect 1 (Low Power, Low Voltage, Power Distribution)
3) Physical System Interconnect 2 (Alternate topologies, Longer Lengths, Higher Device counts)
4) New Connections (VHDCI, SCA)
5) Hot Plugging (expanded specs beyond present)

Taken together, these new areas expand the capabilities of parallel SCSI far beyond that available today.

Except for some techniques used to achieve higher device count there are no significant SCSI software changes needed to realize the benefits.

SERVER SPI
SPI-SVR

The Server SPI area delivers a single interface for both single ended and differential SCSI while offering the performance of FAST 40 and higher data phases. The term "Server" indicates that this type of SCSI would find its most likely applications in high performance servers where the maximum storage bus performance is needed.

A new form of differential interface, based on lower signal levels, different termination, but the same cables, connectors and backplanes as today's SCSI is introduced. This interface uses lower common mode levels and is extendable to higher speeds (eg FAST 80) without changing the chip power dissipation very much.

A single chip protocol implementation, including all differential transceivers AND single ended transceivers in the same chip, provides for a dramatic reduction in the cost compared to today's differential SCSI interface. A small increase in the chip pin count is needed to support the additional differential pins.

By sensing the voltage levels on the DIFF SENSE line, or possibly by other means, the chip can automatically set its interface to either single ended or differential drivers.

The pinout for the low power differential will be changed from that used in today's differential so that the single ended and the differential functions will align with the pins used for the single ended mode.

Because the low power differential interface uses lower signaling levels it is possible that the single segment bus length will be reduced somewhat.

Present status: Project Proposal expected this week (5/8/95) This is a new proposal.

Physical System Interconnect 1
(Low Power, Low Voltage, Power Distribution)
SPI-PSI1

This area addresses new applications created by an industry trend toward low power, low voltage, and extensions beyond that available in SPI of length, power distribution, and small cable size.

This area provides extensions to SPI to permit next generation applications while maintaining a high degree of compatibility with SPI.

Functions which will be available in this area include:

a) Battery powered and lower voltage power supplies
b) Termination schemes that reduce power consumption
c) Enhanced cabling allowing smaller, more flexible implementations
d) Power distribution within the SCSI interconnection schemes
e) Connectivity between enclosures where restrictions exist
f) Potential limitations for maximum input levels when low voltage logic is used

Present Status: Project proposal expected this week (5/8/95) This is a modification of a previous proposal and may or may not be treated as a new proposal.

Physical System Interconnect 2
(Extended length: propagation speed limited, extenders; Extended configurations: mixed SE/DF, isolated segments, LUN bridges)
SPI-PSI2

This area addresses new applications created by an industry trend toward more complex configurations having one or more of the following features: mixed type, higher device count, isolated segments with branches, and

extended lengths allowed by full use of the presently allowed cable propagation times and the use of extender devices.

This area provides extensions to SPI to permit next generation applications while maintaining a high degree of compatibility with SPI.

Functions which will be available in this area include:

a) Basic reinterpretation of the SCSI-2/SCSI-3 SPI length limits caused by cable propagation speed
b) Point to point and lightly populated length limits allowed by single ended operation (far beyond that allowed in SPI)
c) Configurations allowed by the use of extender/isolator devices: topologies with coupled segments, redundant paths to devices
d) Configurations allowed by the use of low cost, low overhead bridge devices: full use of the LUN for greater device count, initialization schemes, inititor/target placements

Present status: project proposal expected this week (5/8/95) This is a new proposal for a technical report.

SCSI Physical Connections
SPI-SPC

This area addresses new applications created by an industry trend toward more smaller and more integrated connectors and retention schemes.

This area provides extensions to SPI to permit next generation applications while maintaining a high degree of compatibility with SPI.

Functions which will be available in this area include:

a) External connections based on the VHDCI connections (allows up to 4 external wide connections on a single PC option slot and a single port on a PCMCIA card)
b) External connections using a single connector for multiple busses
c) Internal connections based on the SCA connector family (allows a single connector for power, options, and wide bus)

Present status: Project proposal expected this week (5/8/95) This is a new proposal.

SCSI Hot Plugging
SPI-HP

This area addresses new applications created by an industry trend toward more dynamic configurations having one or more of the following features: removable and replaceable devices on active busses, removable and replaceable bus segments in active systems, mixed power conditions in active systems.

This area provides extensions to SPI to permit next generation applications while maintaining a high degree of compatibility with SPI. Although some information is included in SPI for removal and replacement of devices the entire process, including the protocol requirements, are not specified. SPI-HP will complete the specifications and incorporate appropriate references to SPI-PSI1 and SPI-PSI2.

Functions which will be available in this area include:

a) Specification of the compete process and requirements for removing and replacing devices on an active SCSI bus
b) Specification of the complete process and requirements for removing, replacing, and adding bus segments to active SCSI systems

c) Specification of the power distribution requirements for dymanic configurations

Present status: Project proposal expected this week (5/8/95) This is a modification of a previous project proposal and may or may not need to be considered as a new project.

Bill reported that he and Paul Aloisi have been working on the low-power, and that he and Jim McGrath are working on other topologies. Skip Jones questioned the need for so many separate projects. He felt that five projects will fragment the customer preceptions of the end result. He strongly requested that a single project be used. In the end, Skip's request was (mostly) honored. The group agreed to draft a project proposal for a single standards project, called SPI-2. A project proposal for a technical report on Expanded System Physical Configuration (ESPC) was also drafted by Bill after the meeting.

4.2 Power Distribution

Paul Aloisi presented a slide showing functional lengths of TERMPWR distribution from a single source to a terminator at the far end. The content of the slide was as follows:

Power, Smaller Cables and Termpwr Sources - Power Distribution.
Single Ended

TERMPWR		Narrow						Wide			
Source/end V		1-28	1-30	1-32	2-28	2-30	2-32	4-28	4-30	4-32	# Cond - AWG
2.8	2.7	5	3.2	2	10	6.4	4	11.36	7.26	4.6	Feet
4.25	2.7	77.1	49.2	30.9	154.2	98.4	61.8	176.1	112.5	70.7	Feet
4.25	4.0	12.4	7.9	5.0	24.8	15.8	10	28.4	18.2	11.4	Feet

Terminator Input voltage
Maximum cable length in Feet

Termpwr V		1-28	1-30	1-32	2-28	2-30	2-32	4-28	4-30	4-32	
2.8	2.7	1.52	0.98	0.61	3.05	1.95	1.22	3.46	2.2	1.4	Meters
4.25	2.7	23.5	15	9.4	47	30	18.8	53.69	34.3	21.6	Meters
4.25	4.0	3.78	2.4	1.52	7.56	4.8	3.05	8.66	5.55	3.5	Meters

Terminator Input voltage
Maximum cable length in Meters
1 & 2 wires are (18 lines with 12 low maximum)
(2 wire uses the same pin, but two wires crimped together to reduce the drop.)
4 wires is wide (27 lines with 21 low maximum)

Not included:
- Add connector resistance 25 milliohms per mated connector.

Connectors 0.025 ohms per mated connector
Worst case 15 connectors 0.375 ohms
Typical 3 connectors 0.075 ohms
15 connectors will not work (without 4 wire) (4 paralleled con)

The successful operation lengths varied wildly. Several issues were raised regarding the presentation. (The text above has been corrected for some of them.) It was noted that the numbers do not account for losses in connectors. Also, John noted that the numbers assume a single-ended bus.

4.3 Power Dissipation

John reported on the power dissipation numbers developed at the April meeting. He asked if anybody present had problems with the power dissipation numbers. Some of those present were not happy with the 1 watt dissipation proposed at the April meeting. However, they accepted the fact that no lower alternatives were evident.

4.4 Determining Differential vs Singled-ended

John reported on the DiffSense conclusions from the April meeting. With three conditions and four possible DiffSense states, it was thought that using another DiffSense line should be workable. Bill noted that because DiffSense is a single-ended signal, the ground offset levels might be tested instead if the system really had bad ground offset voltages present.

This whole strategy hit a major snag later in the meeting when it was noted by Gene Milligan that SCA connectors do not have an extra line for the second DiffSense line. See item 4.6 for the resolution.

4.5 Propogation Delay Length Limit [Ham]

Bill led an effort to formulate the cable length limit based on propogation delays. He started with the proposition that the maximum allowed one way propogation time is 200 nanoseconds. If propogation speed is T_{pd}, then the cable length limit is $L = 200 / T_{pd}$. Questions were raised about the effects of device delays. Bill adjusted the formula to $L = (200-T_{dd})/T_{pd}$, where T_{dd} is the total device delays.

The idea was to change the normative reference from 25m to 200 nanoseconds, and add an implementor's note that 200 nanoseconds can be conservatively be thought of as 120 feet. There was discussion of whether a technical report or annex is needed. The need for a technical report was based on a desire for quick dissemination of the information. The discussion concluded that a technical report was too big a hammer for the need and that this information could be included in SPI-2.

4.6 Pin-out Definitions

The group discussed the options for pin definitions that will allow devices to differentiate between single-ended and differential bus operation. The first-step solution that seemed to work was to make the terminator drive pin 29 to about its high limit (around 2 volts).

To create the new pin outs, all DB- lines have equivalent DB+ lines on their neighbor conductor. Also, conductor 29 becomes the Low-Power DiffSense (LPDF). Finally, all the ATN- ... I/O- lines have equivalent ATN+ ... I/O+ lines added on their neighbor conductor. This plan held well until questions were raised about SCA environments where another DiffSense line is not available.

After some really interesting digressions, the problems were resolved by requiring the low-power differential terminators to drive the DiffSense line to +1.5V plus or minus 0.1V. This is lower than the current DiffSense voltage level when nothing but RS-485 devices are present. Devices can detect LPDF buses if the DiffSense line is within the voltage range of 0.8 V to 2.2 V. Voltage levels below 0.8 V indicate single-ended and above 2.2 V indicate RS-485 differential.

LPDF devices would be required to disable their drivers if they detect an RS-485 bus. If an LPDF device detects a single-ended bus, it may either:

a) disable its drivers or
b) switch into single-ended mode, if it is capable of both modes of operation.

5. Meeting Schedule

The next meeting of SPI-2 Study Group will be July 10, 1995, in Colorado Springs, CO at the Red Lion Inn (719-576-8900), hosted by Symbios Logic Inc.

6. Adjournment

The meeting was adjourned at 4:00 p.m. on Monday May 8, 1995.