A Proposal for Command Overlap and Command Queuing for ATA Devices

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1 Introduction

This document describes a method for supporting command overlap and command queuing for ATA devices. The goals for the development of this method were:

- Simplest possible protocols to implement.
- Ability to operate on the same cable with legacy devices (i.e., ATA-2 and ATAPI devices).
- Best possible future performance.

No effort was made to preserve existing hardware, firmware or software. Choices were made to provide the simplest, least overhead protocols.

A device implementing this method shall power-up in legacy mode and behave as defined in the ATA-2 specification today. The host may then determine the capabilities of the attached devices and enable the overlap and queuing functionality, if desired.

The protocols are designed to require the minimum possible overhead when both devices on the bus implement the overlap and queuing functionality and allow host DMA engines to provide high performance with minimum hardware.

2 Configurations Supported

Three configurations are supported by this proposal.

2.1 Legacy Configurations

Since the devices implementing this new functionality power up in legacy mode, they may be operated in legacy mode if desired. Therefore, a configuration may be as shown in Figure 1. In this configuration one or both of the devices may be capable of command overlap and queuing but a legacy host will operate them as shown. They operate just as ATA devices operate today where a command on one device is executed completely before a command can be issued to the other device.

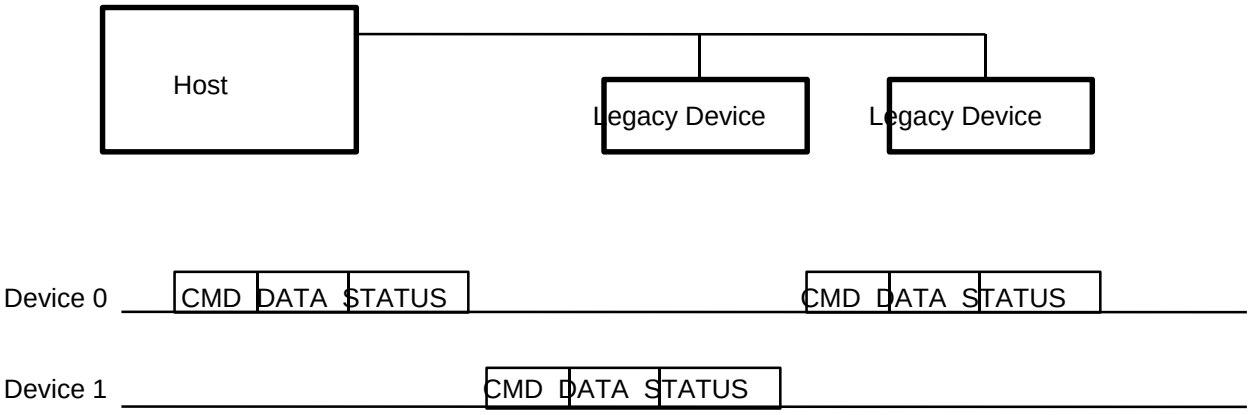


Figure 1 - Legacy Configuration

2.2 Mixed Configurations

The mixed configuration allows one device on the bus to behave as a legacy device while the other device is operating in overlapped/queuing mode as shown in Figure 2. This allows a host that is capable of supporting overlap/queuing to make use of the functionality even when a legacy device incapable of the functionality is present. Figure 2 shows how commands for the two devices may be interleaved when Device 0 is the Legacy Device and Device 1 is the Overlapped Device. One restriction imposed by this proposal is that for mixed configurations, the device performing overlap must be device 1. If the system is configured with the legacy device as Device 1 and the device capable of overlap as Device 0, the system must operate with both devices in legacy mode as described in clause 2.1.

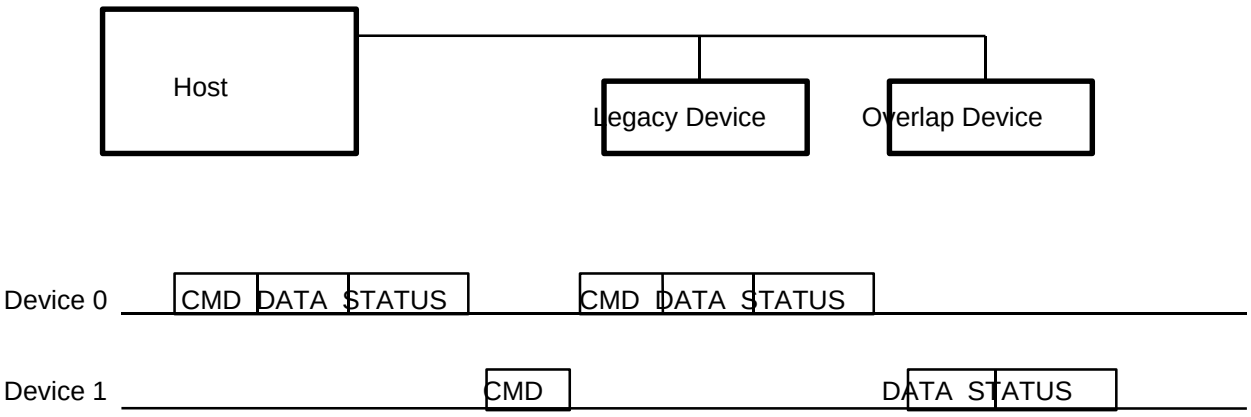


Figure 2 - Mixed Configuration

2.3 Overlapped Configuration

The overlapped configuration can occur when the host and both devices are capable of overlapped functionality as shown in Figure 3 . This proposal is designed to provide minimum overhead and maximum performance with this configuration. As shown by the first command to each device, the issuing of a command to a second device can be placed between the issuing of a command to the first device and the transfer of the first device data. If the device supports queuing as well as overlap, a subsequent commands may be issued to a device before a first command completes as shown by the second and third commands to device 0. In addition, if the data transfer is made in DMA mode, the data transfer may be completed in multiple data transfers instead of a single transfer as shown.

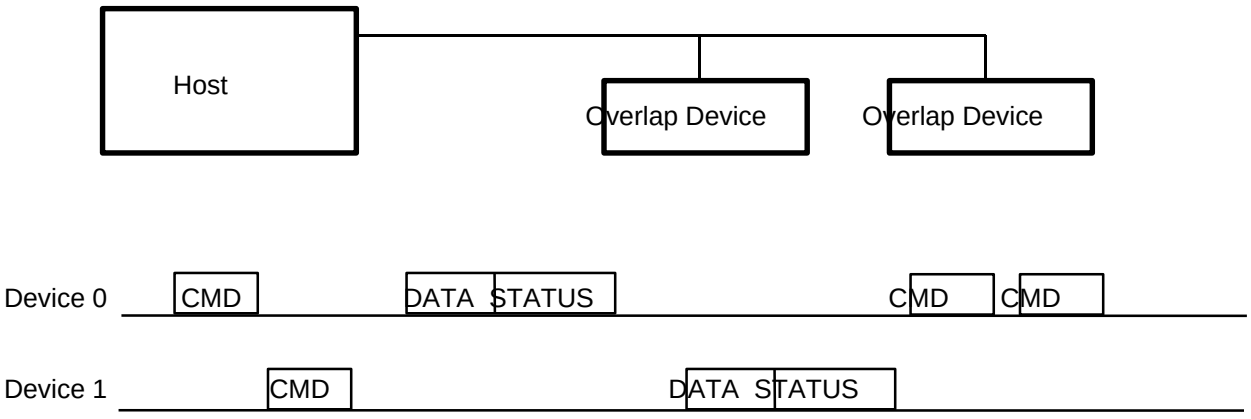


Figure 3 - Overlapped Configuration

3 Overlap/queuing Functional Issues

To implement command overlap and queuing a number of functional issues must be addressed. This clause describes each of these issues and defines solutions to them.

3.1 Register Ownership

Under the ATA specification today, register ownership is very clear. When a command is issued to a device, the device maintains a state with either BSY or DRQ asserted until the command is completed. During this time, the busy device owns the register set and the host may not write registers to either device without dire consequences. When the device has completed the command (neither BSY nor DRQ set), the host owns the registers and may write the registers for either device.

For devices implementing overlap/queuing the rules change slightly. When a command is issued to such a device BSY is asserted as in the legacy case. If the command is a non-data transfer command, BSY remains asserted until the command completes but if both devices support overlap, the host may select the other drive as soom as the command has been written. If the command is a data transfer command, the device sets BSY, inhibits writing of its command block registers, saves the contents of the applicable command block registers, and then clears BSY. If both devices support overlap, the host may select the other device as soon as the command has

been written. If the device supports queuing, the host may issue a second command as soon as BSY is cleared.

If the configuration is a Mixed Configuration, the host must obey the rules that each device expects. That is, if a command is issued to the legacy device, that legacy device own all registers until that command completes. The host may not access the other device. If the host issues a command to the overlapped device, the host may select the legacy device and issue it a command as soon as the overlapped device has cleared BSY.

3.2 Device Selection

Legacy devices today are selected by the host writing the DEV bit in the Drive/Head register. Since this register is owned by a device with BSY or DRQ set, the host is prohibited from selecting the other device when one device is in the process of executing a command.

In legacy or mixed configuration modes, a device capable of command overlap/queuing is selected just as in legacy mode. Since this device will clear its BSY bit as soon as the command parameters have been saved on a data transfer command, a host may then select the legacy device by writing the Drive/Head regsiter and execute a command while the overlap device is working on its data transfer command.

In an overlapped configuration where both devices are in overlap mode, selection is accomplished by a redefinition of the DASP- line. This line becomes DASP-/DSEL. When a device is in legacy mode, the line behaves as DASP- as defined today. When a device is set into overlap mode, it is done so with a qualifier that tells the drive whether or not to use the DSEL line for selection (i.e., for overlapped configurations DSEL is enabled).

Thus in the overlapped configuration, since both devices lockout writes to their command block registers when BSY is set and only accept writes when they are selected, a host may change the device selection at any time it is not actively transferring data or accessing a register. The timing for the operation for the DSEL signal will be exactly the same as the timing for the current CS[1:0]- signals so that a device has those setup and hold times.

3.3 Interrupt Reporting

Today, there is only one INTRQ signal. It is not sharable so that a device can only assert INTRQ when it is selected by the DEV bit. When placed in overlap mode, a new device implementing this function will use either the existing INTRQ line, or a redefined PDIAG-/INTRQ1 line. That is, when in overlap mode, Device 0 will interrupt using INTRQ; Device 1 will interrupt using PDIAG-/INTRQ1. These interrupts may be asserted at any time regardless of whether or not the device is currently selected. As can be seen, this allows the devices to notify the host that service is required regardless of current selection and allows the host to know exactly who is interrupting.

The use of the PDIAG-/INTRQ1 signal results in two limitations. First, in a mixed configuration, the overlapped device must be Device 1 so that its interrupt is distinguishable from that of the legacy device. If the overlapped device is configured as Device 0 and the legacy device as Device 1, the host must operate the overlapped device in legacy mode.

Second, the EXECUTE DEVICE DIAGNOSTICS command may not be issued by the host when any device is in overlapped mode. If the host wishes to issue an EXECUTE DEVICE DIAGNOSTICS command it must first return all overlapped devices to legacy mode.

3.4 Command Queue Tags

The Identify Device info returned by a device capable of overlap/queuing operation will contain a three bit queue depth field. If this field is 0h, the device does not support queuing. If the field contains any other value, this value plus one indicates the depth of queue supported up to a maximum queue depth of eight. Any command tag issued by the host with a tag number greater than this value will cause the command to be aborted.

When issuing a data transfer command to a device in overlapped/queuing mode, a field in the features register will indicate that this is an overlapped command and provide the queue tag number for this command.

When a queued device interrputs for service for a queued command, the tag for the command requiring service will be contained in bits 7, 5 and 4 of the Device/Head register.

All queued commands shall be simple queued data transfer commands, no priority is implied. Only data transfer commands shall be queued and they shall all be of the same type, i.e., shall all be either PIO or DMA transfers. The issuing of a transfer commnad of a different type or the issuing of a non-data transfer command when a queue exists shall cause the entire queue to be aborted.

4 Protocols

The following clauses describe the protocols for operation of devices in overlapped/queued mode.

4.1 Power-up/ Reset Protocol

Devices supporting overlap/queuing functionality shall power-up in legacy mode following the currently specified power-up protocol. These devices shall remain in legacy mode until commanded to enter overlap mode and shall be capable of full normal legacy operation.

4.2 Entering/Leaving Overlapped Mode

To place a device into overlapped mode, the host issues a SET FEATURES command with the set overlapped mode code in the Features register. This code indicates the device should enter overlapped mode and indicates whether or not the DESL signal should be used for selection.

Once placed into overlapped mode, the device shall remain in overlapped mode until:

- a SET FEATURES command is received removing the device from overlaped mode.
- a hardware reset is received.
- the device is powered-down.

These events also cause any existing queue to be aborted.

A software reset does not remove the device from overlapped mode but does abort any existing queue.

4.3 Device Selection

When placed into overlapped mode the device will be instructed whether to enable or disable the use of the DASP-/DSEL signal. In either case, when in overlapped mode a device shall only write from the bus to its command block registers when selected.

4.3.1 Selection with DSEL disabled

When configured in a mixed configuration the overlapped device shall be configured as Device 1 and shall be set to overlaped mode/DSEL disabled. In this state, device selection shall be made via the DRV bit in the Drive/Head register. In this mode, device selection is accomplished just as in legacy mode. However, when data transfer commands are recieved, an overlapped device in this mode shall clear BSY as soon as the required command parameters have been saved from the comand block registers, and therefore, the host may select the other drive as soon as BSY is negated.

4.3.2 Selection with DSEL enabled

When configured in an overlapped configuration, the overlapped devices may be configured as either Device 0 or Device 1 and shall be set to overlapped mode/DSEL enabled. In this mode, device selection is accomplished by the use of the DSEL line.

Timing for the DSEL lines shall provide the same setup and hold times as Address (i.e., DA[2:0] and CS[1:0]) for register accesses and PIO data transfers, and the same setup and hold times as DMACK for DMA data transfers.

The host may change the device selection via DSEL when the currently selected device has BSY asserted. It may change the selection via DSEL when DRQ or DMARQ is asserted but the data transfer has not begun (i.e., no data has been written or read since the assertion of DRQ or DMARQ). However, if DRQ or DMARQ is asserted and data has been transferred since their assertion, the data transfer shall be completed (i.e., DRQ and DMARQ both negated) before selection shall be changed.

When placing a device into overlapped mode/DESL enabled, the host must insure that the DSEL signal is placed in the state selecting the device being given the SET FEATURES command to place it in this state before issuing the command.

4.4 Register Accesses

Protocol for register accesses for a device in overlapped mode changes only slightly from that of legacy operation. When BSY or DRQ are asserted, the information returned when reading a register is undefined except for BSY and DRQ. Registers may be written any time BSY is not set. When a non-data transfer command is issued, BSY shall remain set until the command is completed. When a data transfer command is issued BSY will remain set only until the device has saved the command and its required parameters. When not selected, a device shall ignore all register accesses on the bus.

4.5 PIO Data Transfers

When a PIO data transfer command is recieved, the device will set BSY, prevent all register writes, save the command and required parameters, then clear BSY and again allow register writes. If the device supports command queuing, a new command may be written; if the device does not support command queuing, the writing of a second command will cause the first command to abort.

When the data transfer can be accomplished, the device shall assert DRQ and assert its interrupt, either INTRQ or INTRQ1. If the data transfer can be accomplished immediately upon recieving the command (e.g., a write command and a write buffer is available or read command the the data is available in the device buffer), DRQ may be asserted before BSY is negated. In this case, the host may chose to execute the data transfer imediately or select the other device.

When the device has completed the requested data transfer, the device shall clear DRQ, set CC (Coomand Complete), assert ERR if applicable, and assert its interrupt, either INTRQ or INTRQ1.

When the host receives an interrupt from a device with a PIO data transfer command outstanding, it shall select the interrupting device using the protocol described above. Note that the host explicitly knows which device asserted the interrupt. The host shall then read the Status register.

- If the Status register has DRQ set and BSY cleared, the device is ready to execute the data transfer. At this time, the host may either execute the data transfer or select the other device. If the host chooses to transfer the data, the data is transfered using the existing PIO data transfer protocol. The host shall not deselect the device until the data transfer has been completed.

- If the Status register has DRQ and BSY both cleared and CC set, the device has completed the command. This may be an error free completion or a completion with error depending on the state of the ERR bit just as with a legacy device.

4.6 DMA Data Transfers

When a DMA data transfer command is recieved, the device will set BSY, prevent all register writes, save the command and required parameters, then clear BSY and again allow register writes. If the device supports command queuing, a new command may be written; if the device does not support command queuing, the writing of a second command will cause the first command to abort.

When the data transfer can be accomplished, the device shall assert DMARQ and DRQ, and assert its interrupt, either INTRQ or INTRQ1. If the data transfer can be accomplished immediately upon recieving the command (e.g., a write command and a write buffer is available or read command the the data is available in the device buffer), DMARQ and DRQ may be asserted before BSY is negated. In this case, the host may chose to execute the data transfer imediately or select the other device.

When the device has completed the requested data transfer, the device shall clear DMARQ and DRQ, assert CC, assert ERR if applicable, and assert its interrupt, either INTRQ or INTRQ1.

When the host receives an interrupt from a device with a DMA data transfer command outstanding, it shall select the interrupting device using the protocol described above. Note that the host explicitly knows which device asserted the interrupt.

- If the device has the DMARQ signal asserted, the device is ready to execute the data transfer. At this time, the host may either execute the data transfer or select the other device. If the device has a command queue outstanding the host shall read the Device/Head register to determine the command associated with this service request. If the host chooses to transfer the data, the data is transfered using the existing DMA data transfer protocol. The host may break up a DMA transfer in progress by deasserting DMACK with the timing protocol described in legacy mode. Having done this, the host may select the other device. The device may break up a DMA transfer in progress by deasserting DMARQ with the timing protocol described in legacy mode. The host may then wait for DMARQ to reappear or select the other device. When the device breaks a DMA transfer by deasserting DMARQ, the device shall issue its interrupt, either INTRQ or INTRQ1, when DMARQ is reasserted.

- If the DMARQ signal is not asserted, the host shall read the Status register. If the Status register has DRQ and BSY both cleared and CC asserted, the device has completed the command. This may be an error free completion or a completion with error depending on the state of the ERR bit just as with a legacy device. If the device has a command queue outstanding, the host shall read the Device/Head register to determine which command this is the completion status for.

Note: A host that has an intelligent DMA engine and uses DMA data transfers has very simple interrupt handling. The DMA engine can select the interrupting device and check DMARQ. If DMARQ is asserted, the DMA engine executes the data transfer. If DMARQ is not asserted, the DMA engine passes interrupt to the host device driver for command completion processing and the interrupting device is already selected. It should be noted however, that such a host system must synchronize accesses made to devices from the DMA engine with those made by the host device driver since an atomic sequence of accesses is required by both the device driver and the DMA engine for proper operation.

5 ATA Standard Modifications

This clause describes the specific modifications to the existing ATA standard to incorporate Command overlap and command queuing. Added text is shown in *italtics*. Deleted text is shown with crossouts,. These modifications are presented in the order that they appear in the existing standard with clause numbers appearing in X3T10/2008D revision 0.

Clause 3.1 Definitions and Abbreviations - add:

Command overlap - The ability to issue a command to the second device while the first device is in the process of executing a command.

Command queuing - The ability to issue subsequent commands to a device while previous commands have yet to complete.

Command Tag - An identifier associated with a command that allows the host to determine which of a set of queued commands is being executed.

Clause 4.5 1 ATA Driver Types and Required Pull-ups

Table 6

Signal	Source	Driver Type(1)	Pull-up at Host (2)	Pull-up at each Device (2)	Notes
PDIAG_/ *INTRQ1*	Device	TS		10K	*(5)*
DASP-/*DSEL*	Bidir	OC		10K	(5)

Clause 5.1 Signal Summary

Table 7 Interface Signal Names and Pin Assignments

Description	Source	Pin	Acronym
Passed Diagnostics *or Interrupt Request 1*	(1)	34	PDIAG-*/INTRQ1*
Device active or Slave (Device 1) Present *or Device Select*	(1)	39	DASP-*/DSEL*

Table 8 Interface signals - Alphabetical Listing

Signal	Pin
DASP-*/DSEL*	39
PDIAG-*/INTRQ1*	34

Clause 5.2.4 DASP-(Device active, device 1 present)

Becomes: Clause 5.2.4 DSAP-*/DSEL* (Device active, device 1 present, *Device select*)

Add:

When a device is in Overlapped mode with DSEL enabled, this signal is Device Select, DSEL, and is driven by the host to select a device. When asserted Device 0 is selected, when negated Device 1 is selected. The host may chnage the device selected any time that a data transfer is not in progress. Setup and hold timing for the transition of DSEL shall be the same as ADDR Valid for register accesses or PIO data transfer and the same as DMACK- for DMA transfers. A device supproting overlap shall ignore all bus transactions while not selected. However, the overlapped device shall assert INTRQ or INTRQ1 when the device has an interrupt pending and nIEN is cleared regardless of selection.

Clause 5.2.10 INTRQ (Device interrupt) - add:

When in overlapped mode, Device 0 shall assert INTRQ when the device has an interrupt pending and nIEN is cleared regardless of whether or not it is selected. When in overlapped mode Device 1 shall never drive INTRQ.

Clause 5.2.13 PDIAG- (Passed diagnostics)

Becomes: Clause 5.2.13 PDIAG-*/INTRQ1* (Passed diagnostics *or Interrupt request 1)*

Add:

When a device is in overlapped mode, this signal is Interrupt Request 1, INTRQ1. Functionality of this signal is exactly the same as for INTRQ except that it shall be asserted by Device 1 when Device 1 has an interrupt pending and nIEN is cleared regardless of whether Device 1 is selected or not. When in overlapped mode, Device 1 shall never drive INTRQ.

Clause 6.1 Device Addressing Considerations - add:

A device may be placed in overlap mode with DSEL disabled if it shares the bus with a device incapable of supporting overlap. In this case, device select is accomplished using the DEV bit as described above. In this mode, all register accesses except Device/Head register accesses are ignored when the device is not selected.

If both devices on the bus support overlap mode, both will be placed in Overlap mode with DSEL enabled. In this mode, the DEV bit is ignored and the DSEL signal is used to select the devices. In this mode all register accesses are ignored when the device is not selected.

Clause 6.2.7 - Device/Head register - add:

ACCESS RESTRICTIONS: This register shall be written only when BSY and DRQ equal zero. *When not in overlapped mode, the contents shall only be valid on read when BSY and DRQ equal zero. In overlapped mode, tha tag field shall be valid if either DRQ or DMAREQ is asserted.*

FUNCTIONAL DESCRIPTION - add paragraph:

When in overlapped mode with DSEL enabled, device selection is accomplished via the DSEL signal and the DEV bit is ignored. If the device supports command queuing, the queue tag shall be contained in the tag field for the command for which transfer is being requested or status reported.

FIELD/BIT DESCRIPTION - add:

Command Queuing

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
TAG2		*TAG1*	*TAG0*				

- *Bits 7, 5, 4 - When command queuing is supported abd the device is in overlapped mode, the command queue tag is provided to idenitfy the command for which transfer is requested or status is being reported.*

- *All other bits retain the definition as above.*

Clause 6.2.9 Features register - add:

FUNCTIONAL DESCRIPTION - add:

When in overlapped mode, the host shall set the fact that a data transfer command shall execute in overlapped mode for each transfer command. If the device supports command queuing, the queue tag for the command shall also be provided.

FIELD/BIT DESCRIPTION - add:

Command Queuing

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
OM	*r*	*r*	*r*	*r*	*TAG2*	*TAG1*	*TAG0*

Bits 7 - OM when set indicates the command shall be executed in overlapped mode.

Bits 6-3 - reserved

Bits 2-0 - Queue tag for data transfer command.

Clause 6.2.12 Status register - add:

FIELD/BIT DESCRIPTION - add:

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX/*CC*	ERR

- BSY (Busy) - add:

When a command is accepted and the device is in overlapped mode, BSY shall be set as dscribed above, the device shall save the command and applicable parameters contained in command block registers, then clear BSY. This allows the host to select the other device if desired. If the device supports command queuing, another command may be issued to the device as soon as BSY has been cleared.

- IDX*/CC* Index (IDX) is vendor specific. *When in overlapped mode, this bit is Command Complete (CC). It is set upon completion of a command when the status for that command is present in the Status and Error registers. Upon the completion of a read from this register, the CC bit is cleared.*

Add clause:

***7.X** Overlapped/Command Queuing Mode*

7.X.1 Overlapped configurations

Two configurations are supported byoverlapped mode.

7.X.1.1 Mixed Configurations

The mixed configuration allows one device on the bus to behave as a legacy device while the other device is operating in overlapped/queuing mode as shown in X1. This allows a host that is capable of supporting overlap/queuing to make use of the functionality even when a legacy device incapable of the functionality is present. Figure 2 shows how commands for the two devices may be interleaved when Device 0 is the Legacy Device and Device 1 is the Overlapped Device. One restriction is imposed for mixed configurations, the device performing overlap must be device 1. If the system is configured with the legacy device as Device 1 and the device capable of overlap as Device 0, the system must operate with both devices in legacy mode.

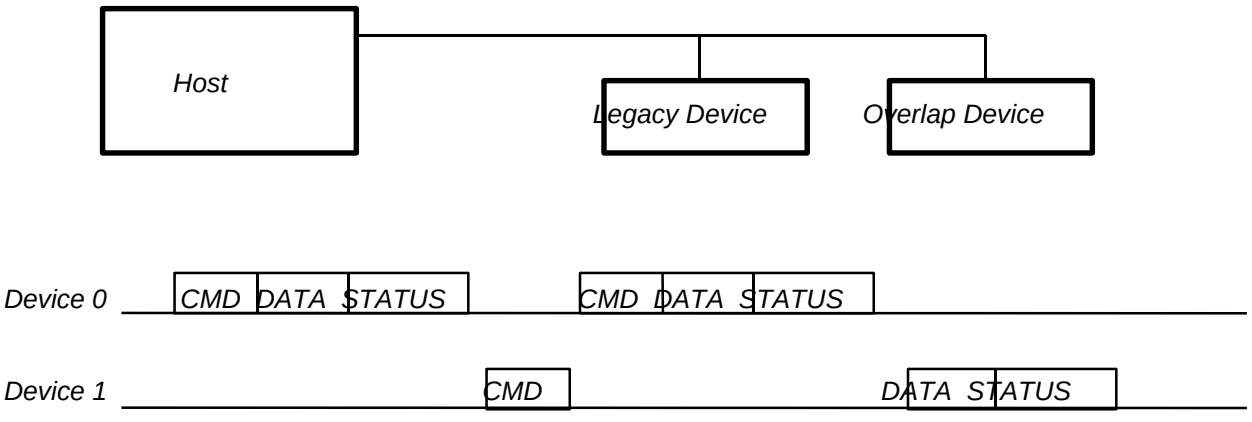


Figure X1- Mixed Configuration

7.X.1.2 Overlapped Configuration

The overlapped configuration can occur when the host and both devices are capable of overlapped functionality as shown in Figure X2. Overlapped mode is designed to provide minimum overhead and maximum performance with this configuration. As shown by the first command to each device, the issuing of a command to a second device can be placed between the issuing of a command to the first device and the transfer of the first device data. If the device supports queuing as well as overlap, a subsequent commands may be issued to a device before a first command completes as shown by the second and third commands to device 0. In addition, if the data transfer is made in DMA mode, the data transfer may be completed in multiple data transfers instead of a single transfer as shown.

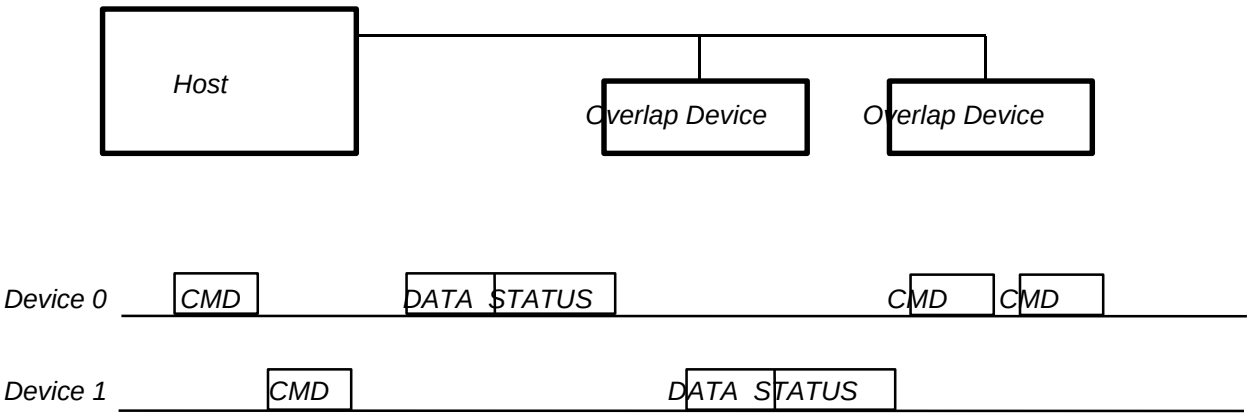


Figure X2 - Overlapped Configuration

7.X.2 Overlapped Register Ownership

When a command is issued to a device in overlapped mode, BSY is asserted. If the command is a non-data transfer command, BSY remains asserted until the command completes but if both devices support overlap, the host may select the other device as soom as the command has been written. If the command is a data transfer command, the device sets BSY, inhibits writing of its command block registers, saves the contents of the applicable command block registers, and then clears BSY. If both devices support overlap, the host may select the other device as soon as the command has been written. If the device supports queuing, the host may issue a second command as soon as BSY is cleared.

If the configuration is a Mixed Configuration, the host must obey the rules that each device expects. That is, if a command is issued to the legacy device, that legacy device own all registers until that command completes. The host may not access the other device. If the host issues a command to the overlapped device, the host may select the legacy device and issue it a command as soon as BSY has been cleared by the overlapped device.

7.X.3 Device Selection

In a mixed configuration, a device capable of command overlap/queuing is selected just as in legacy mode. Since this device will clear its BSY bit as soon as the command parameters have been saved on a data transfer command, a host may then select the legacy device and execute a command while the overlap device is working on its data transfer command.

In an overlapped configuration where both devices are in overlap mode, selection is accomplished with the DASP-/DESL line. When a device is in legacy mode, the line behaves as DASP- as defined today. When a device is set into overlap mode, it is done so with a qualifier that tells the drive whether or not to use the DSEL line for selection (i.e., for overlapped configurations DSEL is enabled).

Thus in the overlapped configuration, since both devices lockout writes to their command block registers when BSY is set and only accept writes when they are selected, a host may change the device selection at any time it is not actively transferring data or accessing a register. The timing for the operation for the DSEL signal will be exactly the same as the timing for the current CS[1:0]- signals so that a device has those setup and hold times.

7.X.4 Interrupt Reporting

When placed in overlapped mode, a device implementing this function will use either the INTRQ line, or the PDIAG-/INTRQ1 line for reporting interrupts. That is, when in overlap mode, Device 0 shall interrupt using INTRQ; Device 1 shall interrupt using PDIAG-/INTRQ1. These interrupts may be asserted at any time regardless of whether or not the device is currently selected. This allows the devices to notify the host that service is required regardless of current selection and allows the host to know exactly who is interrupting.

The use of the PDIAG-/INTRQ1 signal results in two limitations. First, in a mixed configuration, the overlapped device shall be Device 1 so that its interrupt is distinguishable from that of the legacy device. If the overlapped device is configured as Device 0 and the legacy device as Device 1, the host shall operate the overlapped device in legacy mode.

Second, the EXECUTE DEVICE DIAGNOSTICS command shall not be issued by the host when any device is in overlapped mode. If the host wishes to issue an EXECUTE DEVICE DIAGNOSTICS command it shall first return all overlapped devices to legacy mode.

7.X.5 Command Queue Tags

The Identify Device info returned by a device capable of overlap/queuing operation shall contain a three bit queue depth field. If this field is 0h, the device does not support queuing. If the field contains any other value, this value plus one indicates the depth of queue supported up to a maximum queue depth of eight. Any tag issued by the host with a tag number greater than this value shall cause the command to be aborted.

When issuing a data transfer command to a device in overlapped/queuing mode, the tag field in the features register shall indicate that this is an overlapped command and provide the queue tag number for this command.

When a queued device interrputs for service for a queued command, the tag for the command requiring service shall be contained in bits 7, 5 and 4 of the Device/Head register.

All queued commands are simple queued data transfer commands, no priority is implied. Only data transfer commands shall be queued and they shall all be of the same type, i.e., shall all be either PIO or DMA transfers. The issuing of a transfer commnad of a different type or the issuing of a non-data transfer command when a queue exists shall cause the entire queue to be aborted.

Clause 8.8 EXECUTE DEVICE DIAGNOSTICS - add:

PREREQUISITES - *This command shall not be issued to a device in overlapped mode.*

Clause 8.10 IDENTIFY DEVICE - add:

Table 14 - Identify Device Information - add:

Word	F/V	
71	*F*	*15 Overlapped Mode supported* *14-11 Queue depth supported* *10-0 Reserved*
72-127	R	Reserved

Add **clause *8.10.36*** *Word 71: Overlapped Mode/Command Queuing Supported*

Word 71 of the parameter information of the IDENTIFY DEVICE command is defined as the Overlapped Mode/Command Queuing supported field. If bit 15 is set to one, the device supports Overlapped Mode. This mode may be set via a SET FEATURES command.

Bits 14-11 define the queue depth supported if command queuing is supported when in overlapped mode. If 0h is present in this field, the device does not support command queuing. If this field contains a value other than 0h, that value + 1 is the maximum queue depth supported by the device.

Clauses 8.17, 8.18, 8.19, 8.20, 8.21, 8.22, 8.37, 8.38, 8.39, 8.40, 8.41, 8.42, and 8.43 (Data transfer commands) - add:

INPUTS - add sentence:

For devices in overlapped mode, the Features register shall be set to specify that the command is to be executed in overlapped mode. If the device supports command queuing, the command tag shall also be set in the Features register.

Clause 8.32 SET FEATURES add:

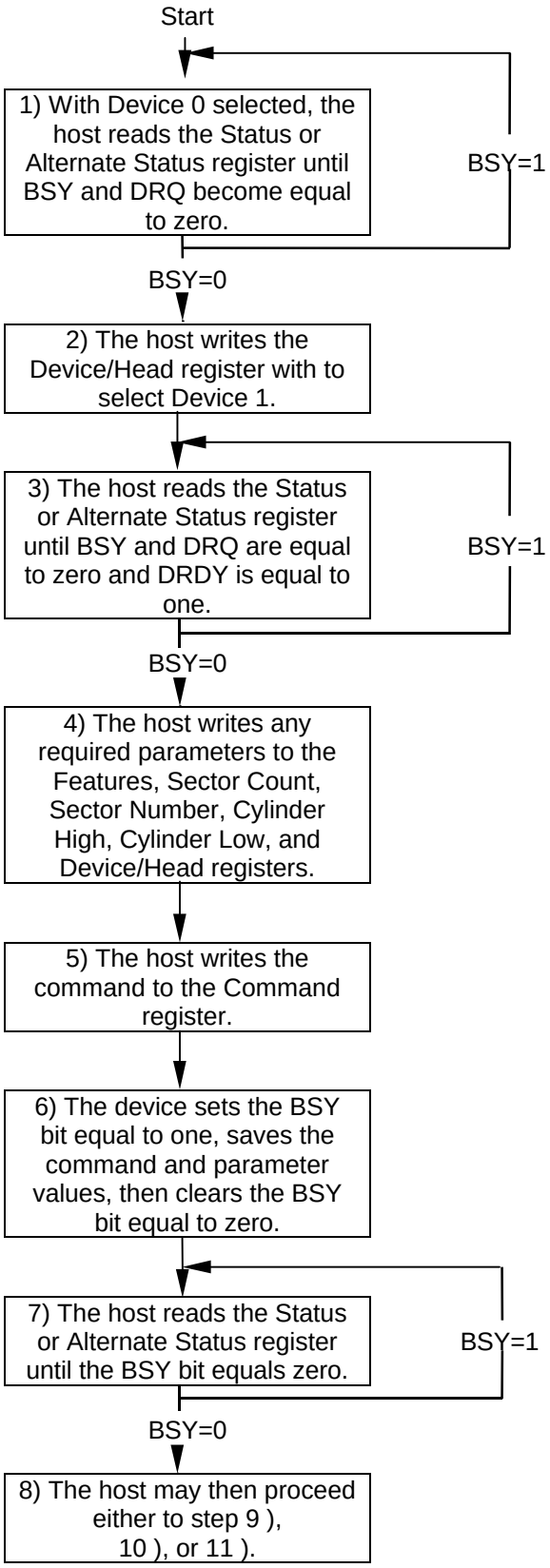
Table 17 - Set Features register Definitions add:

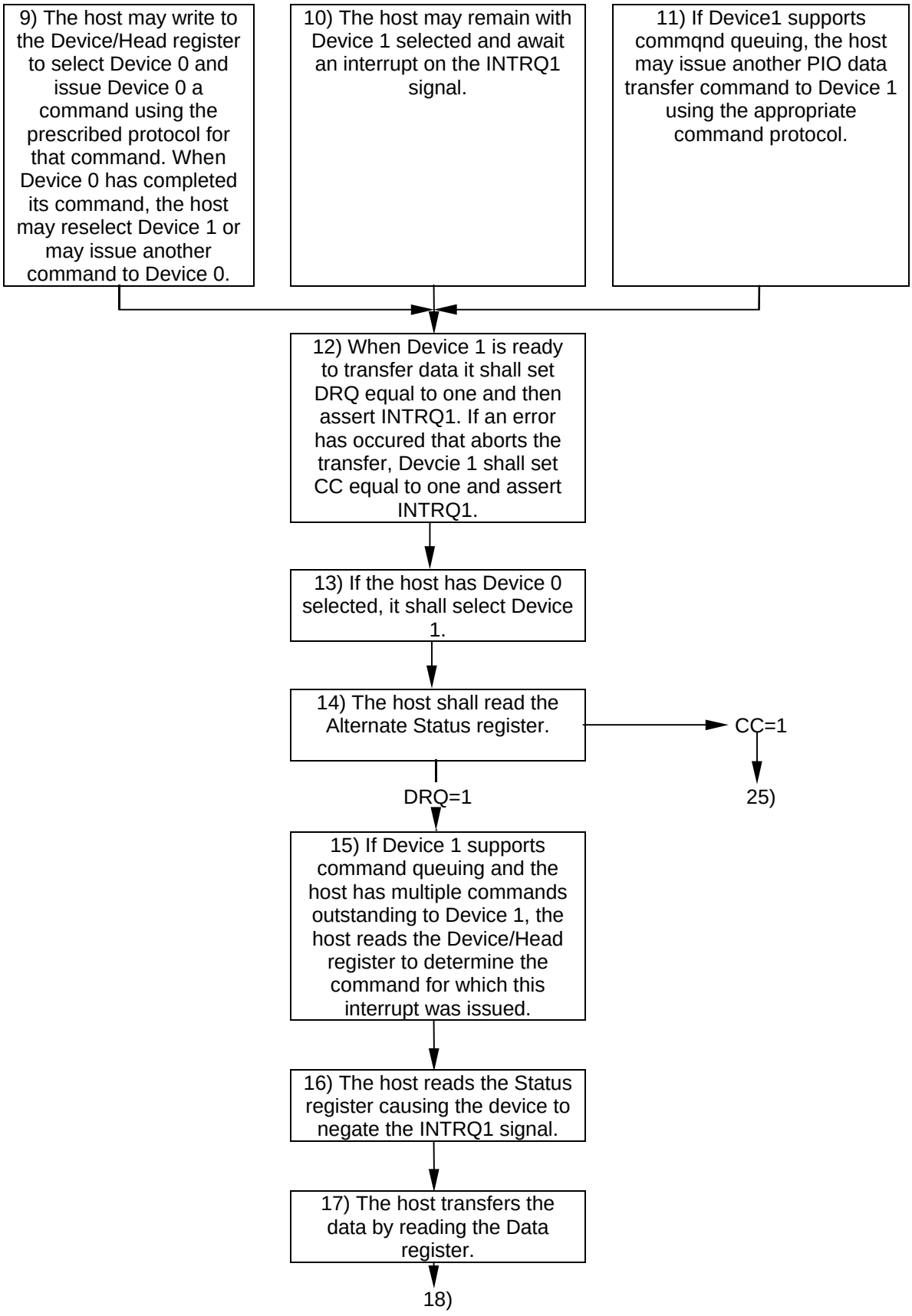
DDh	*Enable overlapped mode with DSEL disabled*
DEh	*Enable overlapped mode with DSEL enabled*
DFh	*Disable overlapped mode*

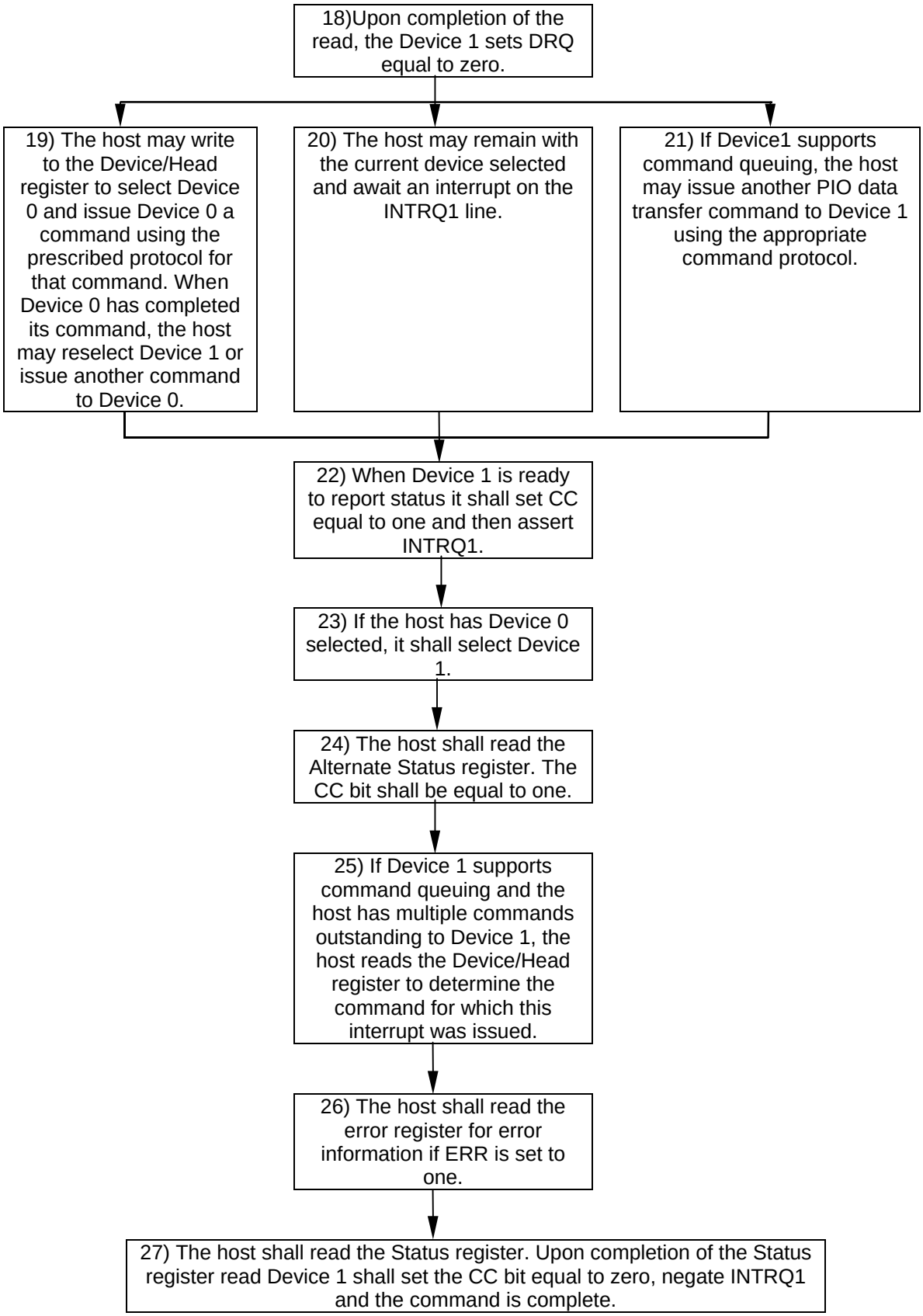
Clause 9.3 PIO data in commands - add:

9.3.1 Overlapped mode/DSEL disabled PIO data in commands

When a mixed configuration exists with one legacy device and one device that supports overlapped mode, the device that supports overlapped mode may be set into overlapped mode with DSEL disabled. In this configuration, the legacy device shall be Device 0 and the overlapped device shall be Device 1. The overlapped device then operates with the following protocol:

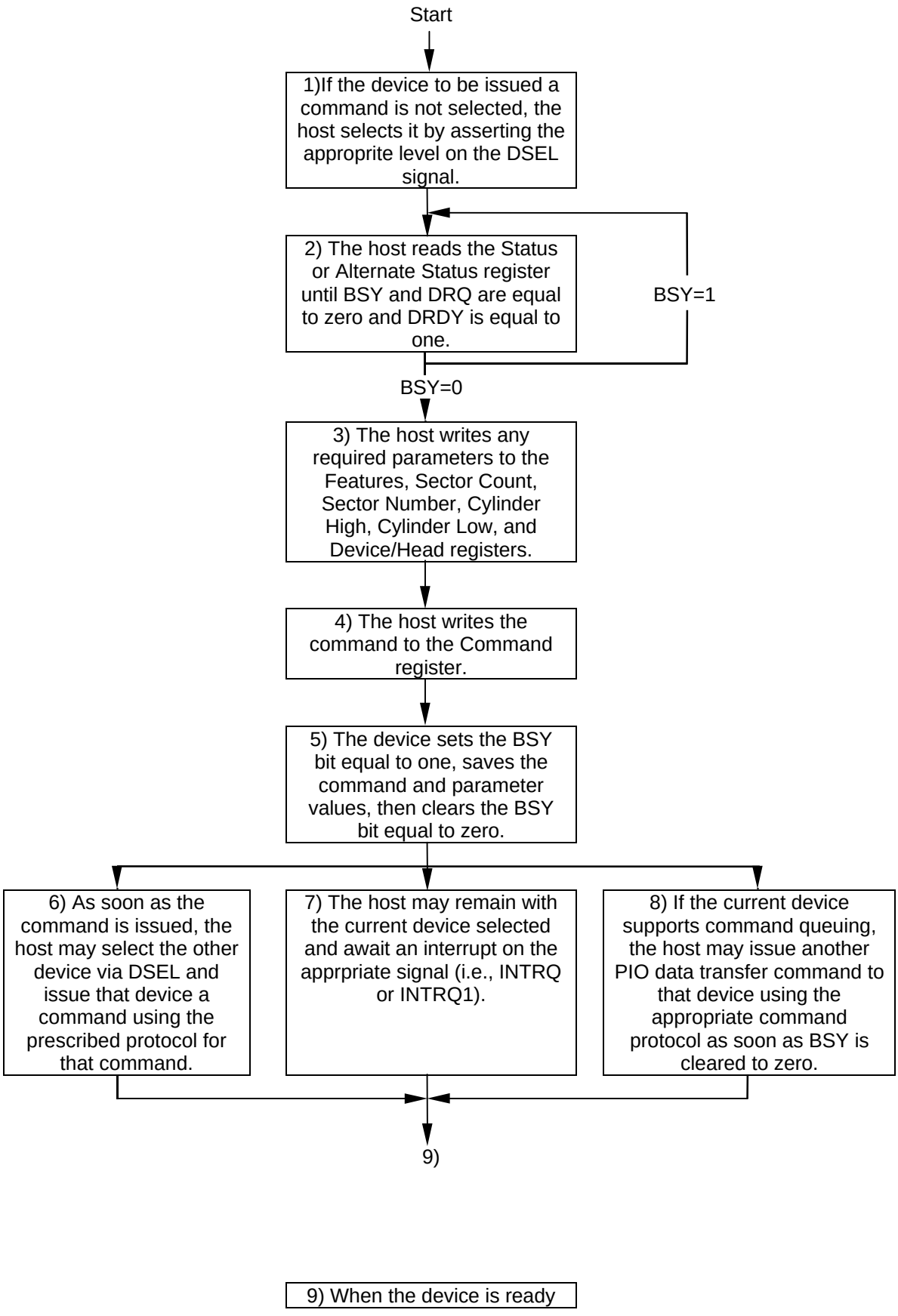

Start
1) With Device 0 selected, the host reads the Status or Alternate Status register until BSY and DRQ become equal to zero.
BSY=1
BSY=0
2) The host writes the Device/Head register with to select Device 1.
3) The host reads the Status or Alternate Status register until BSY and DRQ are equal to zero and DRDY is equal to one.
BSY=1
BSY=0
4) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low, and Device/Head registers.
5) The host writes the command to the Command register.
6) The device sets the BSY bit equal to one, saves the command and parameter values, then clears the BSY bit equal to zero.
7) The host reads the Status or Alternate Status register until the BSY bit equals zero.
BSY=1
BSY=0
8) The host may then proceed either to step 9), 10), or 11).

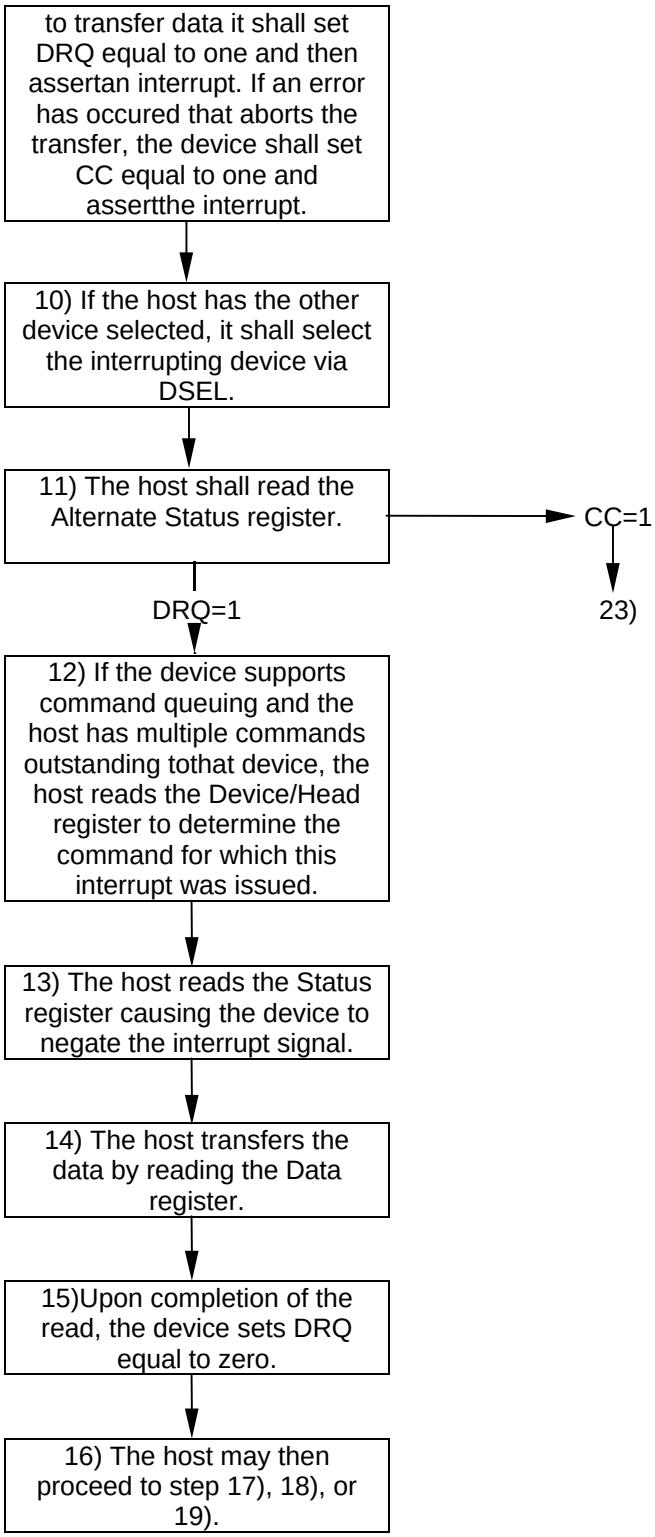

9) The host may write to the Device/Head register to select Device 0 and issue Device 0 a command using the prescribed protocol for that command. When Device 0 has completed its command, the host may reselect Device 1 or may issue another command to Device 0.
10) The host may remain with Device 1 selected and await an interrupt on the INTRQ1 signal.
11) If Device1 supports commqnd queuing, the host may issue another PIO data transfer command to Device 1 using the appropriate command protocol.
12) When Device 1 is ready to transfer data it shall set DRQ equal to one and then assert INTRQ1. If an error has occured that aborts the transfer, Devcie 1 shall set CC equal to one and assert INTRQ1.
13) If the host has Device 0 selected, it shall select Device 1.
14) The host shall read the Alternate Status register.
CC=1
25)
DRQ=1
15) If Device 1 supports command queuing and the host has multiple commands outstanding to Device 1, the host reads the Device/Head register to determine the command for which this interrupt was issued.
16) The host reads the Status register causing the device to negate the INTRQ1 signal.
17) The host transfers the data by reading the Data register.
18)


18)Upon completion of the read, the Device 1 sets DRQ equal to zero.
19) The host may write to the Device/Head register to select Device 0 and issue Device 0 a command using the prescribed protocol for that command. When Device 0 has completed its command, the host may reselect Device 1 or issue another command to Device 0.
20) The host may remain with the current device selected and await an interrupt on the INTRQ1 line.
21) If Device1 supports command queuing, the host may issue another PIO data transfer command to Device 1 using the appropriate command protocol.
22) When Device 1 is ready to report status it shall set CC equal to one and then assert INTRQ1.
23) If the host has Device 0 selected, it shall select Device 1.
24) The host shall read the Alternate Status register. The CC bit shall be equal to one.
25) If Device 1 supports command queuing and the host has multiple commands outstanding to Device 1, the host reads the Device/Head register to determine the command for which this interrupt was issued.
26) The host shall read the error register for error information if ERR is set to one.
27) The host shall read the Status register. Upon completion of the Status register read Device 1 shall set the CC bit equal to zero, negate INTRQ1 and the command is complete.

9.3.2 Overlapped mode/DSEL enabled PIO data in commands

When an overlapped configuration exists with both devices that support overlapped mode, the devices are set into overlapped mode with DSEL enabled. In this configuration, device selection is accomplished via the DSEL signal. The device then operate with the following protocol:

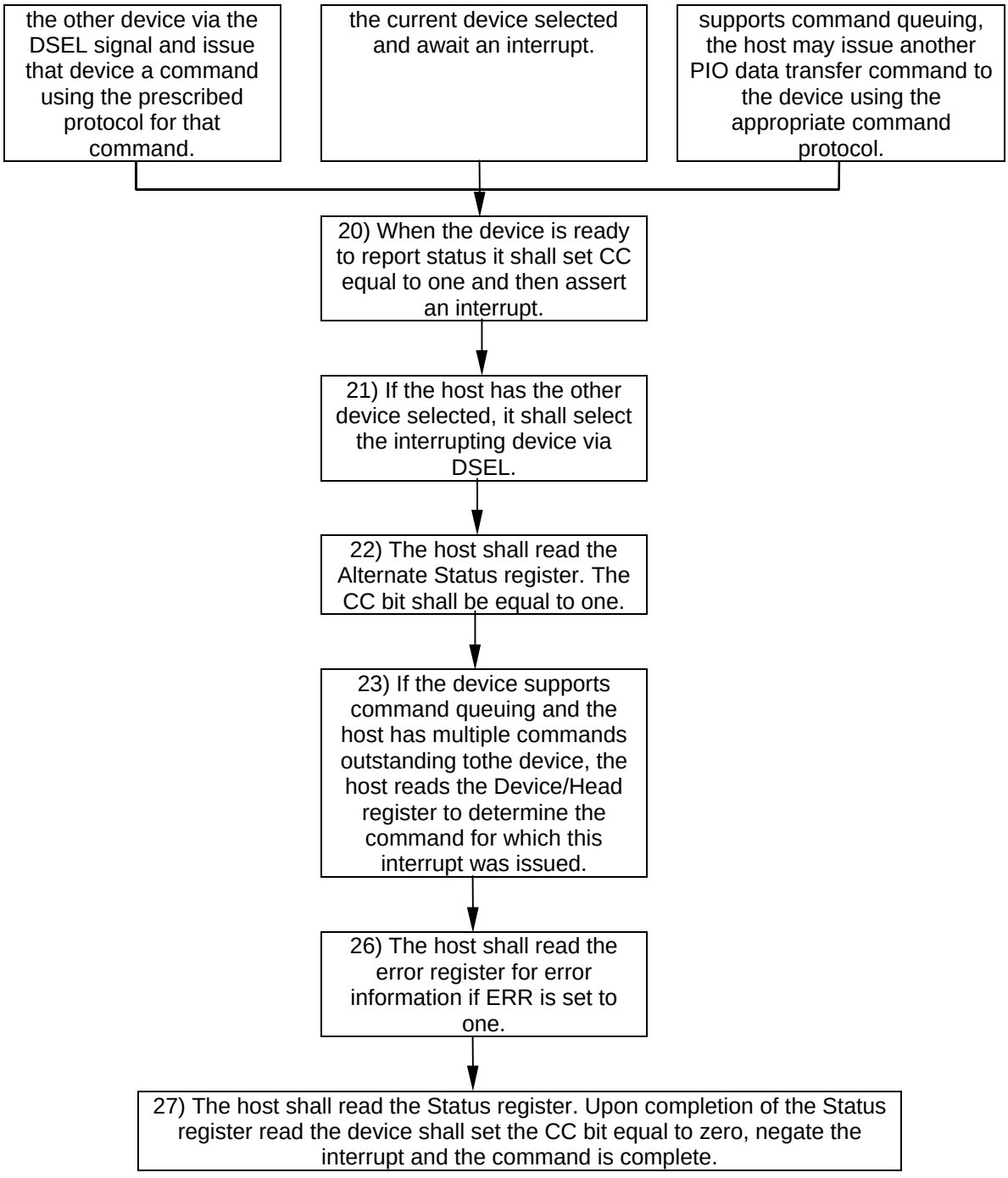

Start
1)If the device to be issued a command is not selected, the host selects it by asserting the approprite level on the DSEL signal.
2) The host reads the Status or Alternate Status register until BSY and DRQ are equal to zero and DRDY is equal to one.
BSY=1
BSY=0
3) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low, and Device/Head registers.
4) The host writes the command to the Command register.
5) The device sets the BSY bit equal to one, saves the command and parameter values, then clears the BSY bit equal to zero.
6) As soon as the command is issued, the host may select the other device via DSEL and issue that device a command using the prescribed protocol for that command.
7) The host may remain with the current device selected and await an interrupt on the apprpriate signal (i.e., INTRQ or INTRQ1).
8) If the current device supports command queuing, the host may issue another PIO data transfer command to that device using the appropriate command protocol as soon as BSY is cleared to zero.
9)
9) When the device is ready



17) The host may select

18) The host may remain with

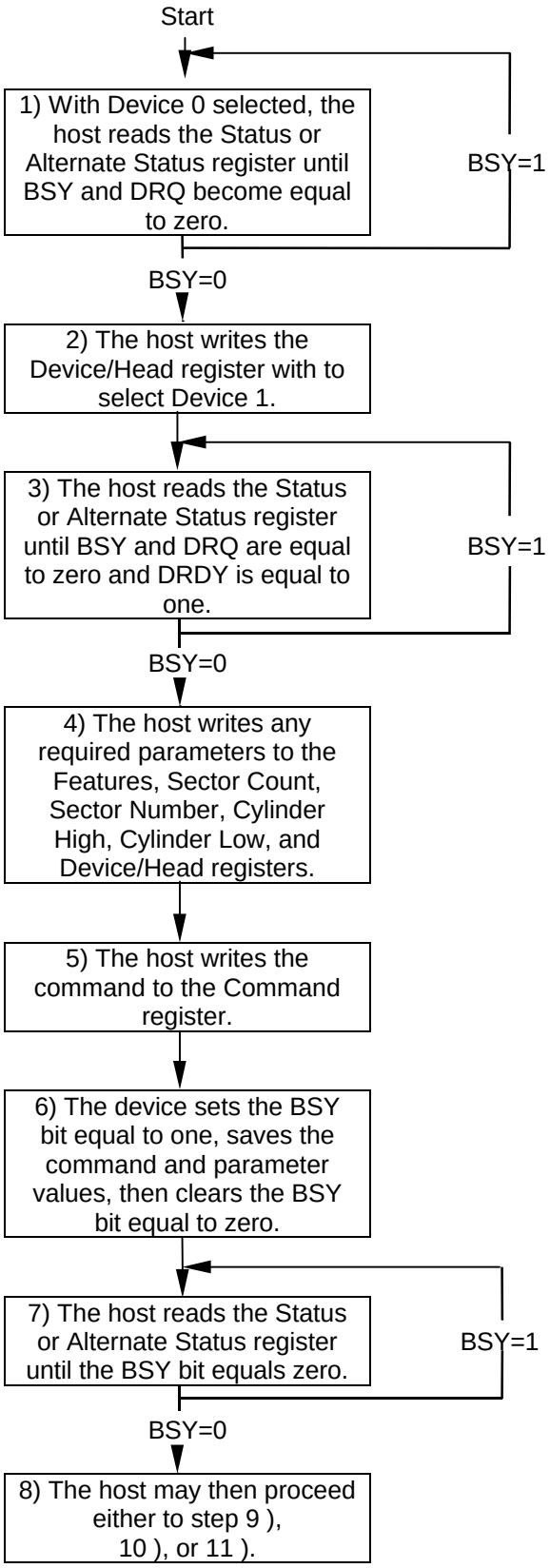
19) If the current device

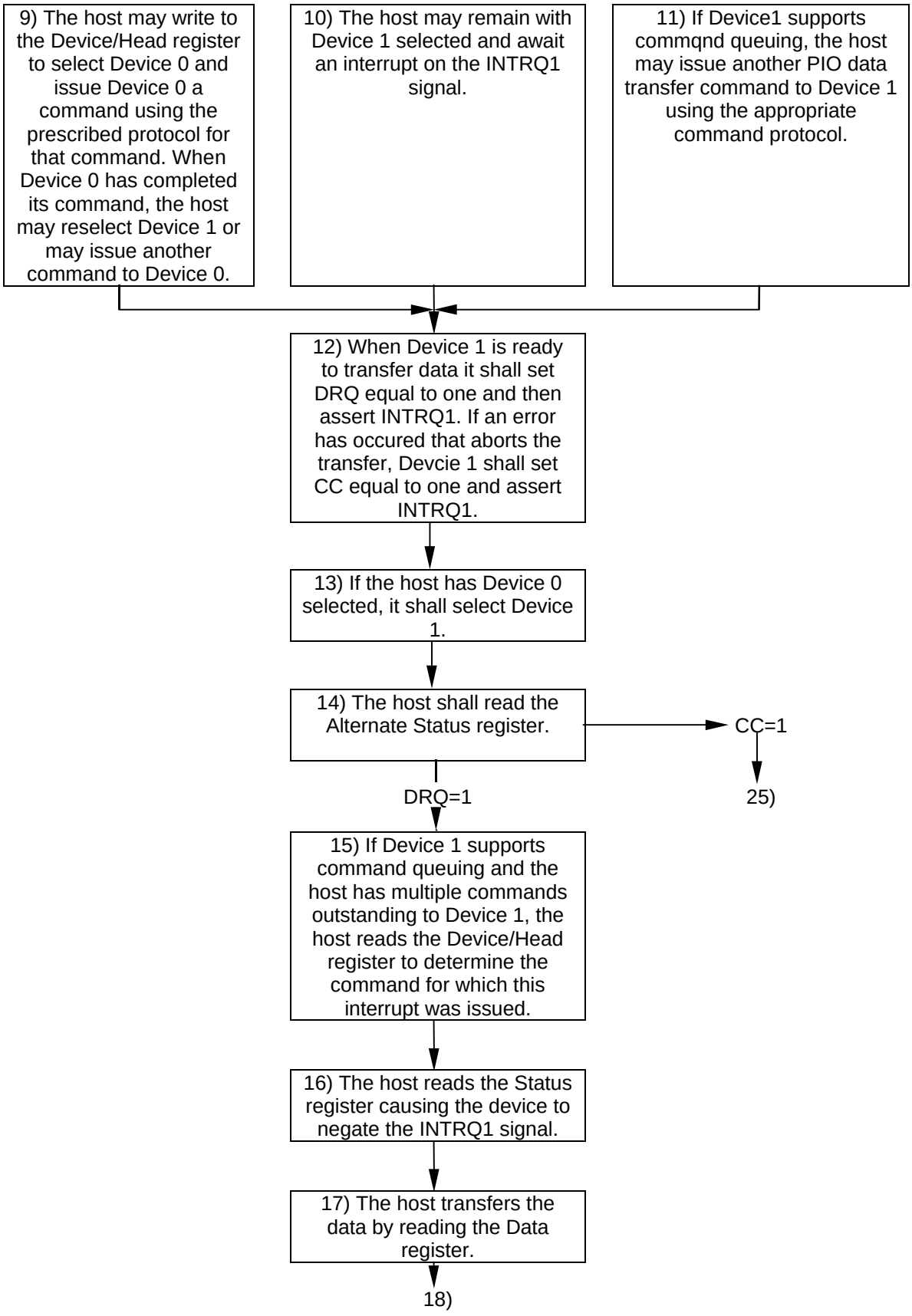

the other device via the DSEL signal and issue that device a command using the prescribed protocol for that command.
the current device selected and await an interrupt.
supports command queuing, the host may issue another PIO data transfer command to the device using the appropriate command protocol.
20) When the device is ready to report status it shall set CC equal to one and then assert an interrupt.
21) If the host has the other device selected, it shall select the interrupting device via DSEL.
22) The host shall read the Alternate Status register. The CC bit shall be equal to one.
23) If the device supports command queuing and the host has multiple commands outstanding tothe device, the host reads the Device/Head register to determine the command for which this interrupt was issued.
26) The host shall read the error register for error information if ERR is set to one.
27) The host shall read the Status register. Upon completion of the Status register read the device shall set the CC bit equal to zero, negate the interrupt and the command is complete.

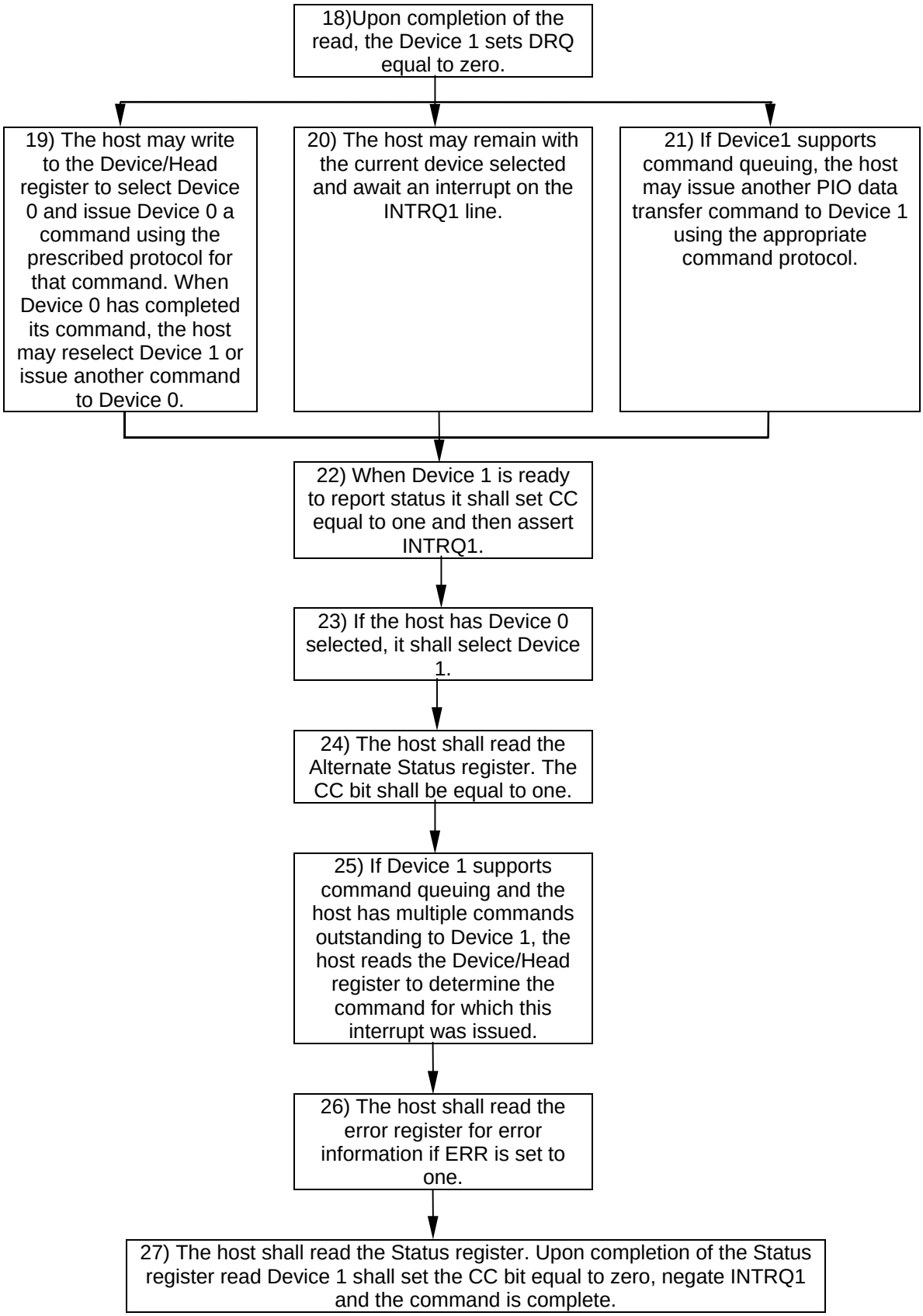
Clause 9.4 PIO data out commands - add:

9.4.1 Overlapped mode/DSEL disabled PIO data in commands

When a mixed configuration exists with one legacy device and one device that supports overlapped mode, the device that supports overlapped mode may be set into overlapped mode with DSEL disabled. In this configuration, the legacy device shall be Device 0 and the overlapped device shall be Device 1. The overlapped device then operates with the following protocol:

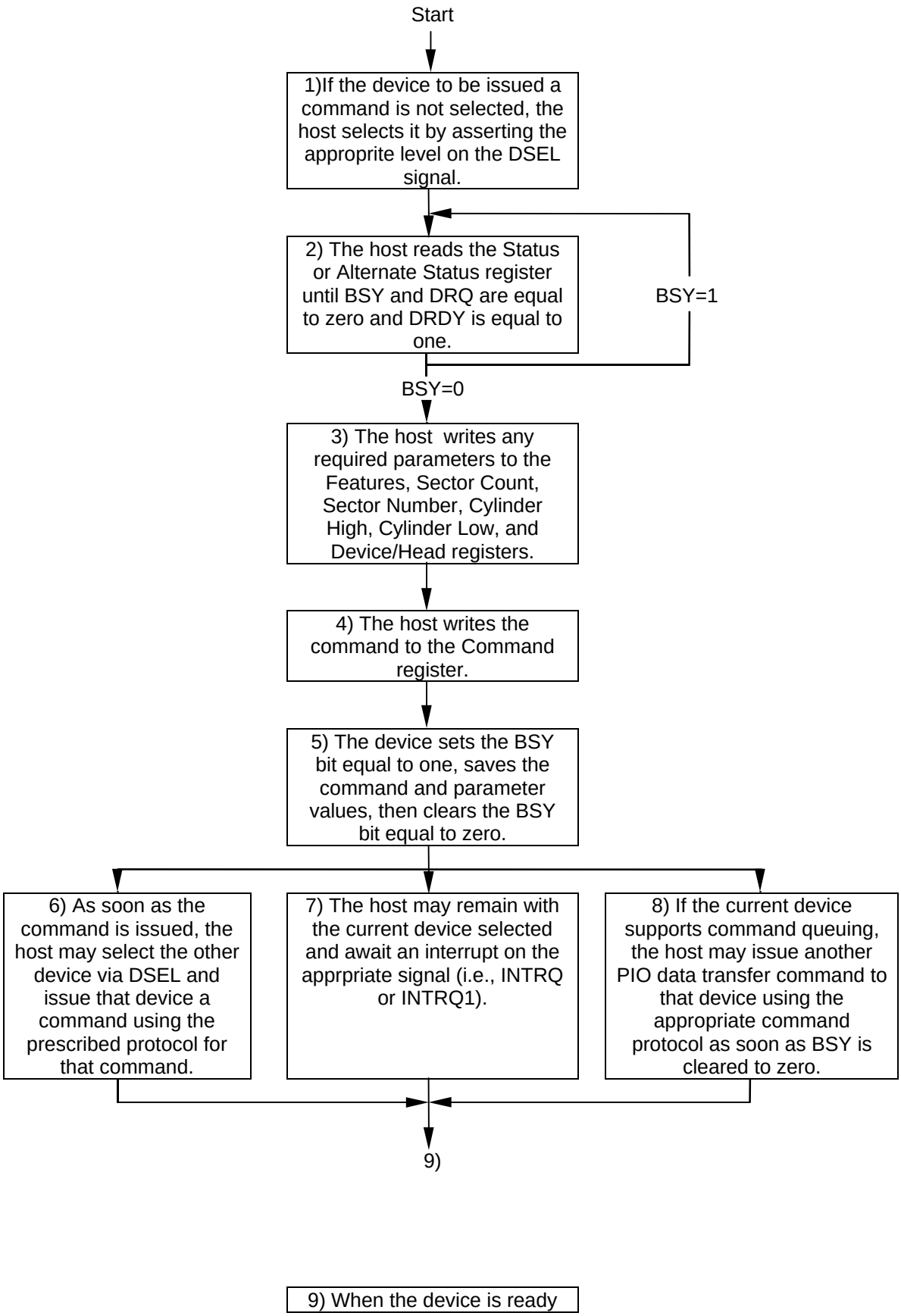

Start
1) With Device 0 selected, the host reads the Status or Alternate Status register until BSY and DRQ become equal to zero.
BSY=1
BSY=0
2) The host writes the Device/Head register with to select Device 1.
3) The host reads the Status or Alternate Status register until BSY and DRQ are equal to zero and DRDY is equal to one.
BSY=1
BSY=0
4) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low, and Device/Head registers.
5) The host writes the command to the Command register.
6) The device sets the BSY bit equal to one, saves the command and parameter values, then clears the BSY bit equal to zero.
7) The host reads the Status or Alternate Status register until the BSY bit equals zero.
BSY=1
BSY=0
8) The host may then proceed either to step 9), 10), or 11).

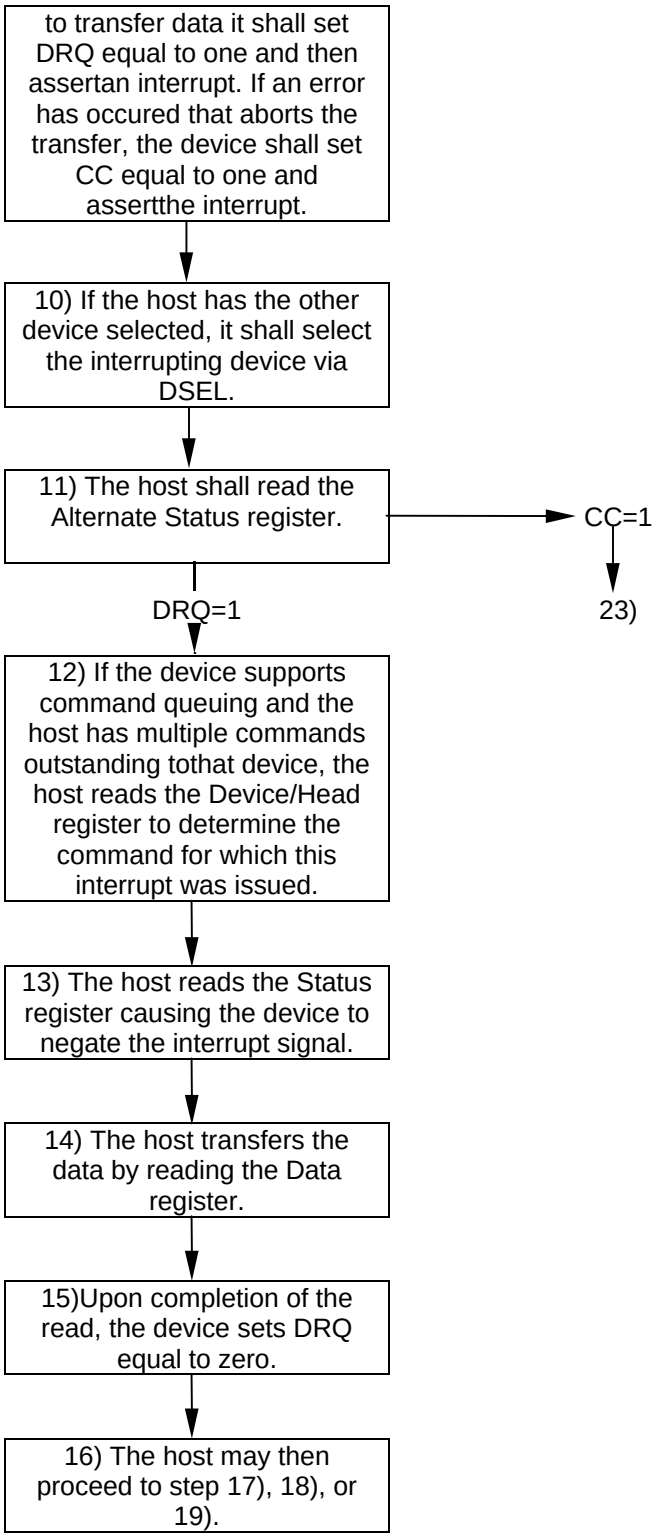

9) The host may write to the Device/Head register to select Device 0 and issue Device 0 a command using the prescribed protocol for that command. When Device 0 has completed its command, the host may reselect Device 1 or may issue another command to Device 0.
10) The host may remain with Device 1 selected and await an interrupt on the INTRQ1 signal.
11) If Device1 supports commqnd queuing, the host may issue another PIO data transfer command to Device 1 using the appropriate command protocol.
12) When Device 1 is ready to transfer data it shall set DRQ equal to one and then assert INTRQ1. If an error has occured that aborts the transfer, Devcie 1 shall set CC equal to one and assert INTRQ1.
13) If the host has Device 0 selected, it shall select Device 1.
14) The host shall read the Alternate Status register.
CC=1
25)
DRQ=1
15) If Device 1 supports command queuing and the host has multiple commands outstanding to Device 1, the host reads the Device/Head register to determine the command for which this interrupt was issued.
16) The host reads the Status register causing the device to negate the INTRQ1 signal.
17) The host transfers the data by reading the Data register.
18)


18)Upon completion of the read, the Device 1 sets DRQ equal to zero.
19) The host may write to the Device/Head register to select Device 0 and issue Device 0 a command using the prescribed protocol for that command. When Device 0 has completed its command, the host may reselect Device 1 or issue another command to Device 0.
20) The host may remain with the current device selected and await an interrupt on the INTRQ1 line.
21) If Device1 supports command queuing, the host may issue another PIO data transfer command to Device 1 using the appropriate command protocol.
22) When Device 1 is ready to report status it shall set CC equal to one and then assert INTRQ1.
23) If the host has Device 0 selected, it shall select Device 1.
24) The host shall read the Alternate Status register. The CC bit shall be equal to one.
25) If Device 1 supports command queuing and the host has multiple commands outstanding to Device 1, the host reads the Device/Head register to determine the command for which this interrupt was issued.
26) The host shall read the error register for error information if ERR is set to one.
27) The host shall read the Status register. Upon completion of the Status register read Device 1 shall set the CC bit equal to zero, negate INTRQ1 and the command is complete.

9.4.2 Overlapped mode/DSEL enabled PIO data in commands

When an overlapped configuration exists with both devices that support overlapped mode, the devices are set into overlapped mode with DSEL enabled. In this configuration, device selection is accomplished via the DSEL signal. The device then operate with the following protocol:

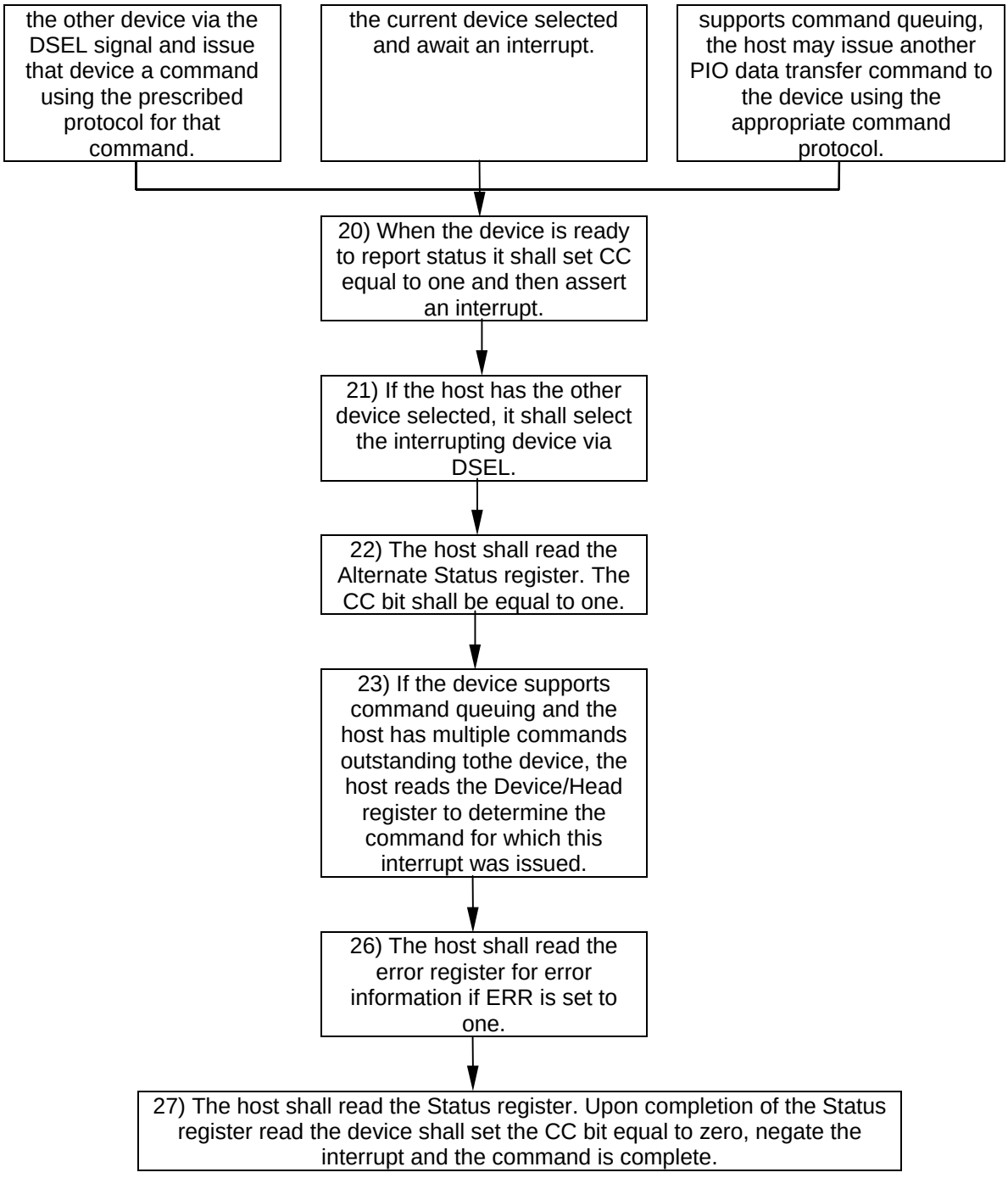

Start
1)If the device to be issued a command is not selected, the host selects it by asserting the approprite level on the DSEL signal.
2) The host reads the Status or Alternate Status register until BSY and DRQ are equal to zero and DRDY is equal to one.
BSY=1
BSY=0
3) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low, and Device/Head registers.
4) The host writes the command to the Command register.
5) The device sets the BSY bit equal to one, saves the command and parameter values, then clears the BSY bit equal to zero.
6) As soon as the command is issued, the host may select the other device via DSEL and issue that device a command using the prescribed protocol for that command.
7) The host may remain with the current device selected and await an interrupt on the apprpriate signal (i.e., INTRQ or INTRQ1).
8) If the current device supports command queuing, the host may issue another PIO data transfer command to that device using the appropriate command protocol as soon as BSY is cleared to zero.
9)
9) When the device is ready



17) The host may select

18) The host may remain with

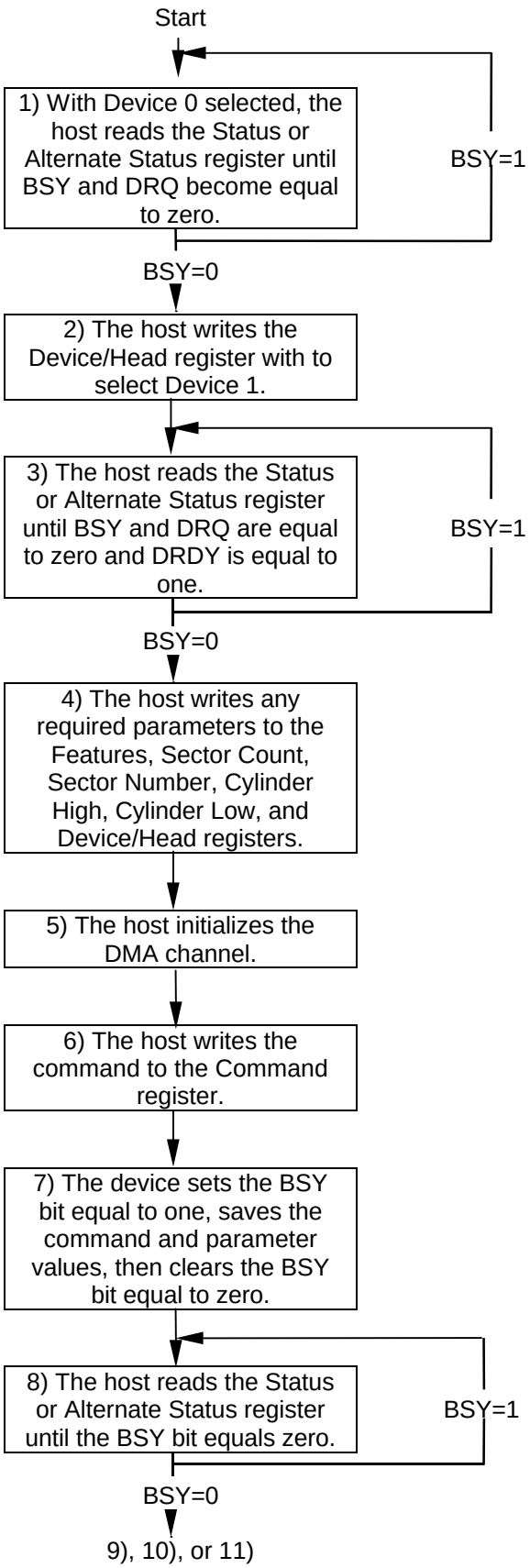
19) If the current device

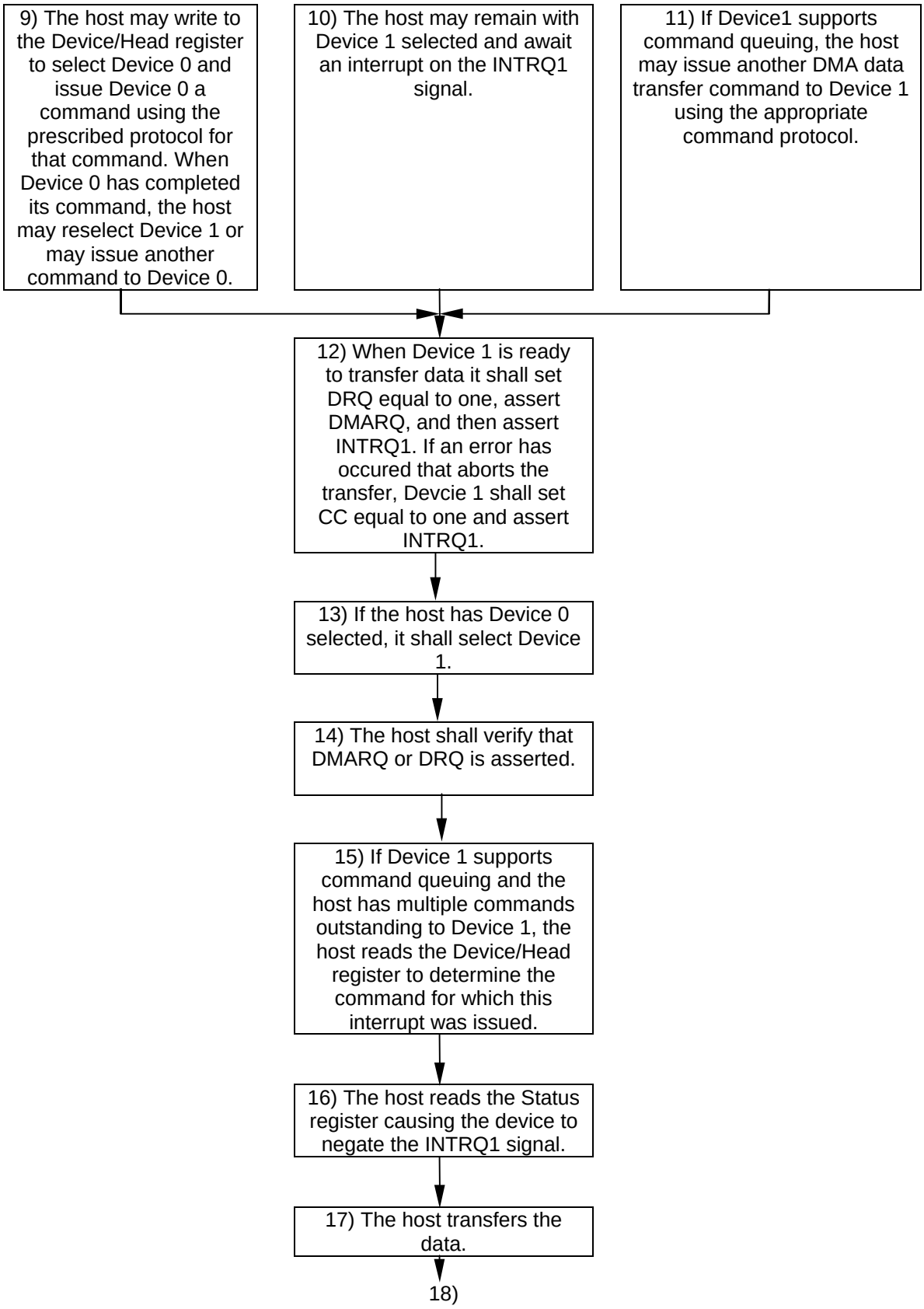

the other device via the DSEL signal and issue that device a command using the prescribed protocol for that command.
the current device selected and await an interrupt.
supports command queuing, the host may issue another PIO data transfer command to the device using the appropriate command protocol.
20) When the device is ready to report status it shall set CC equal to one and then assert an interrupt.
21) If the host has the other device selected, it shall select the interrupting device via DSEL.
22) The host shall read the Alternate Status register. The CC bit shall be equal to one.
23) If the device supports command queuing and the host has multiple commands outstanding tothe device, the host reads the Device/Head register to determine the command for which this interrupt was issued.
26) The host shall read the error register for error information if ERR is set to one.
27) The host shall read the Status register. Upon completion of the Status register read the device shall set the CC bit equal to zero, negate the interrupt and the command is complete.

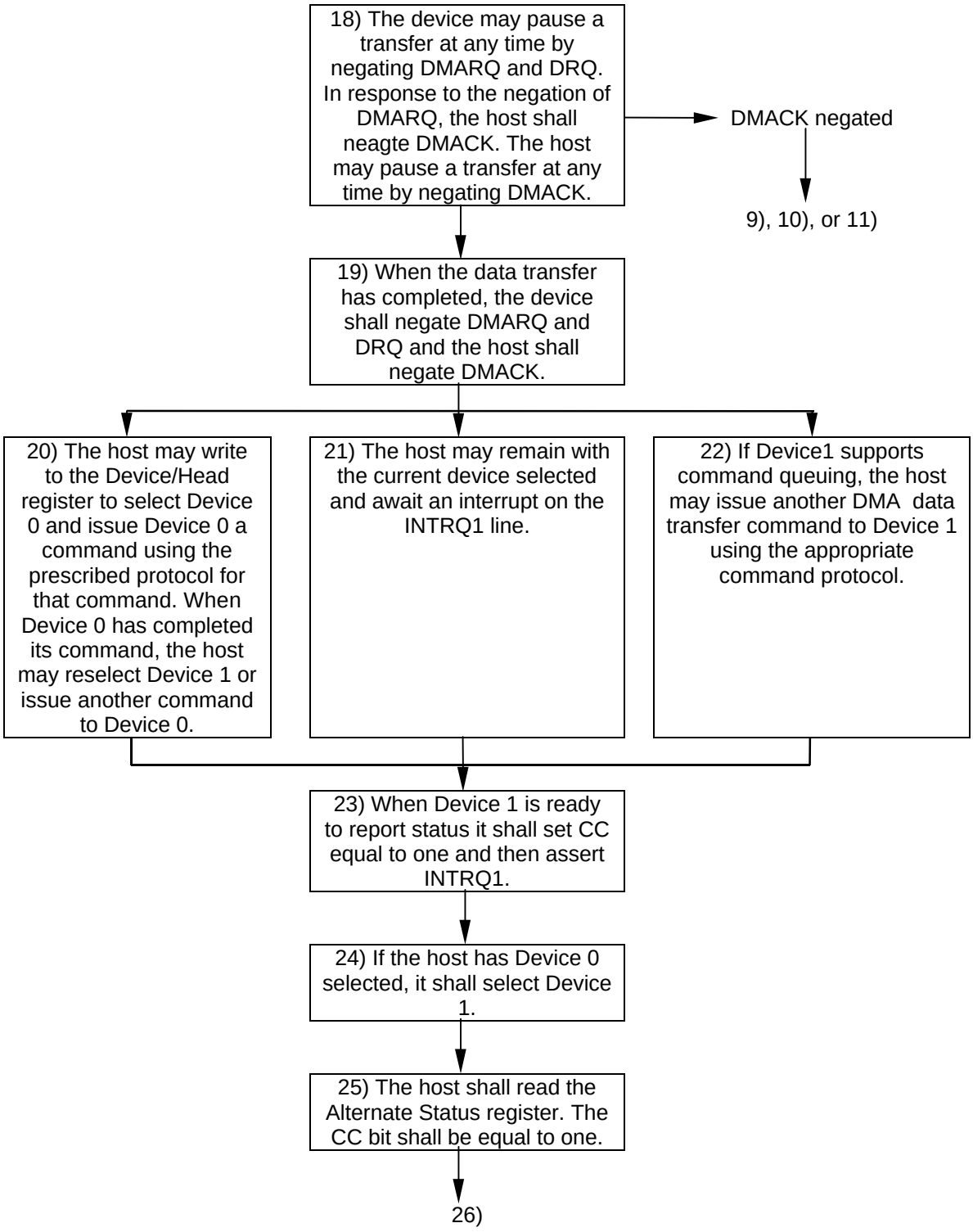
Clause 9.6 DMA data transfer commands - add:

9.6.1 Overlapped mode/DSEL disabled DMA data transfer commands

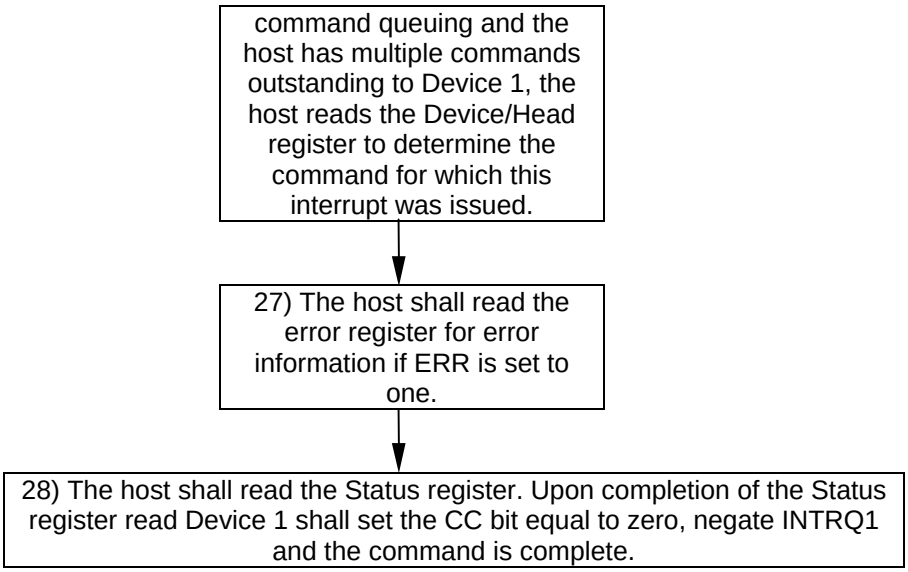
When a mixed configuration exists with one legacy device and one device that supports overlapped mode, the device that supports overlapped mode may be set into overlapped mode with DSEL disabled. In this configuration, the legacy device shall be Device 0 and the overlapped device shall be Device 1. The overlapped device then operates with the following protocol:


Start
1) With Device 0 selected, the host reads the Status or Alternate Status register until BSY and DRQ become equal to zero.
BSY=1
BSY=0
2) The host writes the Device/Head register with to select Device 1.
3) The host reads the Status or Alternate Status register until BSY and DRQ are equal to zero and DRDY is equal to one.
BSY=1
BSY=0
4) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low, and Device/Head registers.
5) The host initializes the DMA channel.
6) The host writes the command to the Command register.
7) The device sets the BSY bit equal to one, saves the command and parameter values, then clears the BSY bit equal to zero.
8) The host reads the Status or Alternate Status register until the BSY bit equals zero.
BSY=1
BSY=0
9), 10), or 11)


9) The host may write to the Device/Head register to select Device 0 and issue Device 0 a command using the prescribed protocol for that command. When Device 0 has completed its command, the host may reselect Device 1 or may issue another command to Device 0.
10) The host may remain with Device 1 selected and await an interrupt on the INTRQ1 signal.
11) If Device1 supports command queuing, the host may issue another DMA data transfer command to Device 1 using the appropriate command protocol.
12) When Device 1 is ready to transfer data it shall set DRQ equal to one, assert DMARQ, and then assert INTRQ1. If an error has occured that aborts the transfer, Devcie 1 shall set CC equal to one and assert INTRQ1.
13) If the host has Device 0 selected, it shall select Device 1.
14) The host shall verify that DMARQ or DRQ is asserted.
15) If Device 1 supports command queuing and the host has multiple commands outstanding to Device 1, the host reads the Device/Head register to determine the command for which this interrupt was issued.
16) The host reads the Status register causing the device to negate the INTRQ1 signal.
17) The host transfers the data.
18)

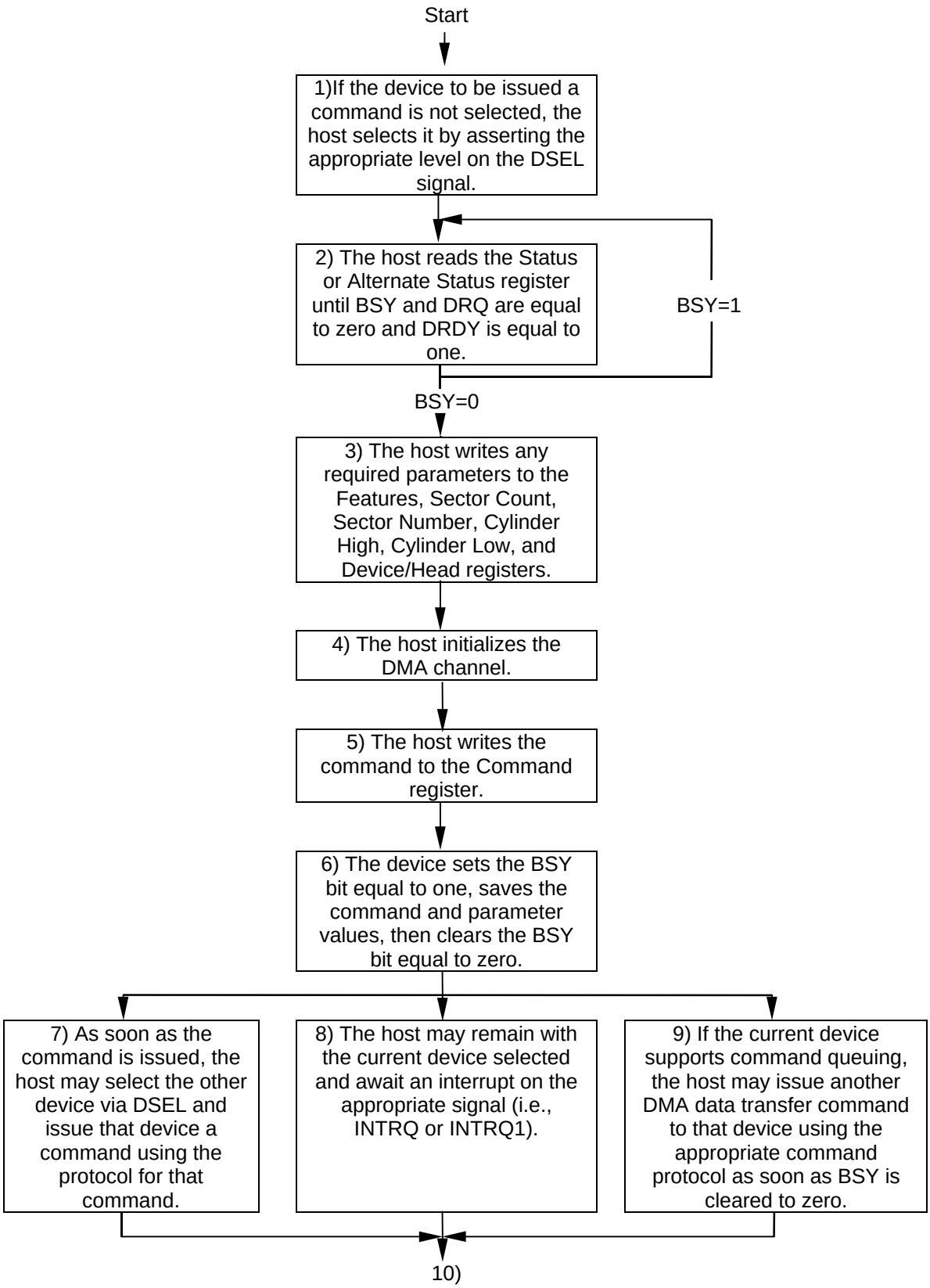


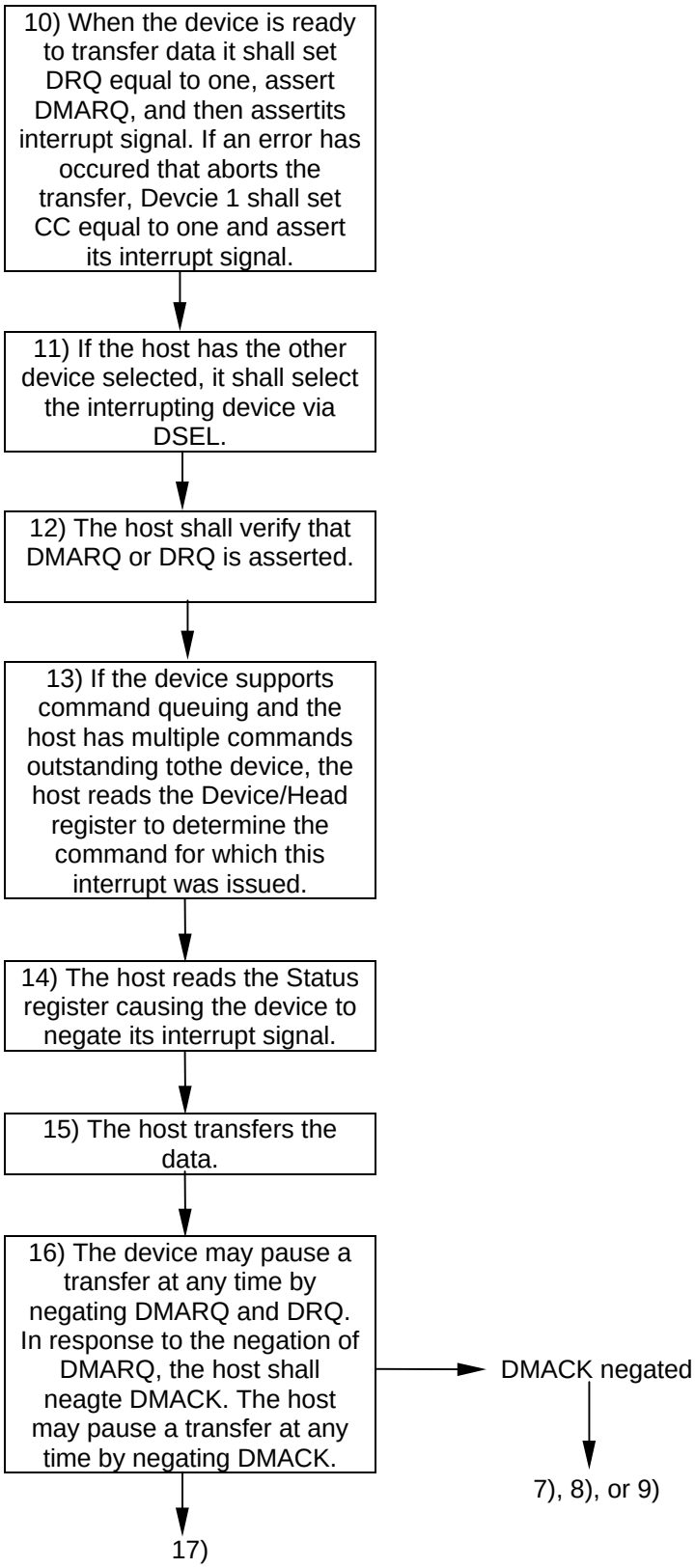
26) If Device 1 supports

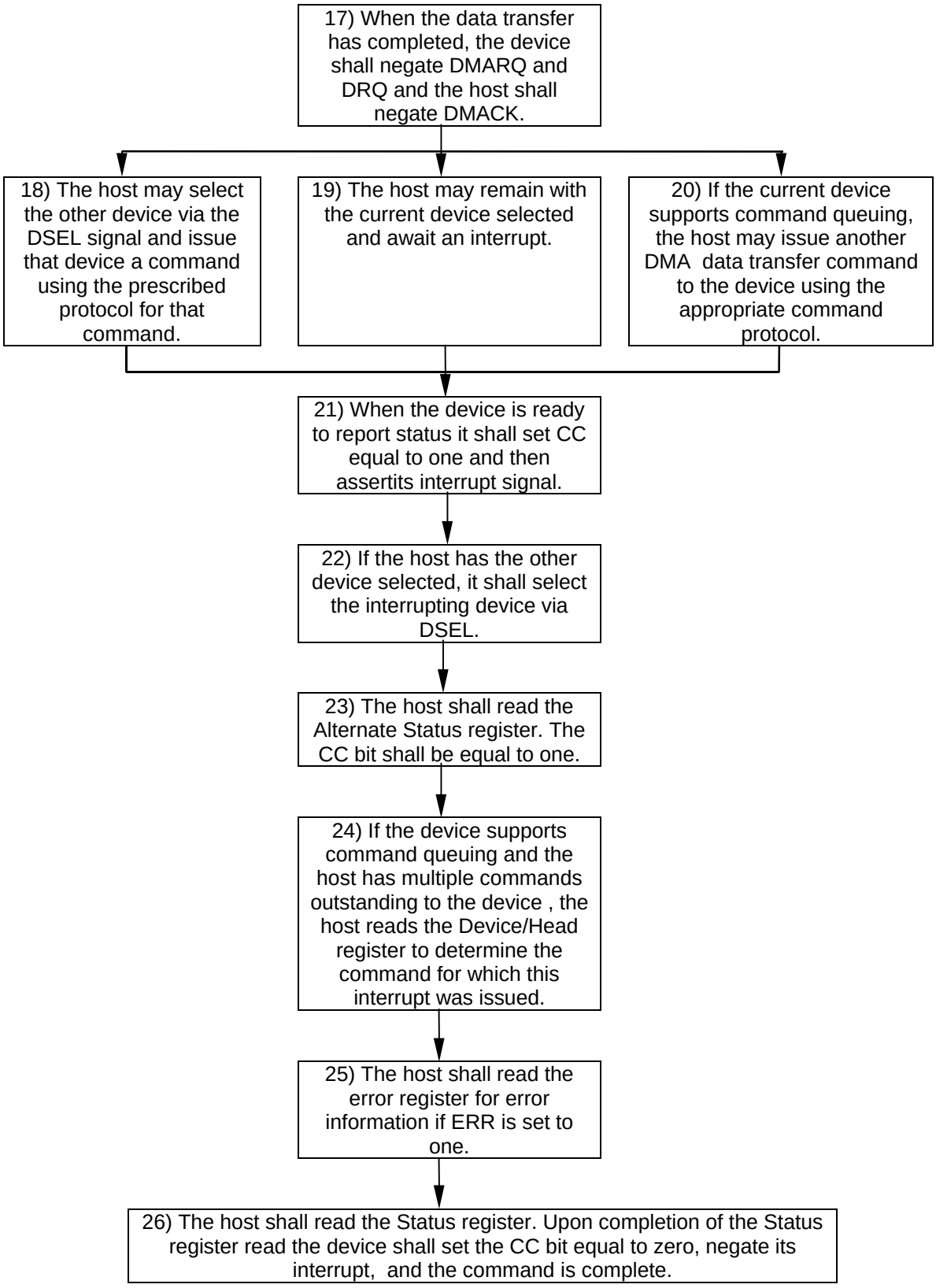


9.6.2 Overlapped mode/DSEL enabled DMA data transfer commands

When an overlapped configuration exists with both devices that support overlapped mode, the devices are set into overlapped mode with DSEL enabled. In this configuration, device selection is accomplished via the DSEL signal. The device then operate with the following protocol:


Start
1)If the device to be issued a command is not selected, the host selects it by asserting the appropriate level on the DSEL signal.
2) The host reads the Status or Alternate Status register until BSY and DRQ are equal to zero and DRDY is equal to one.
BSY=1
BSY=0
3) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder High, Cylinder Low, and Device/Head registers.
4) The host initializes the DMA channel.
5) The host writes the command to the Command register.
6) The device sets the BSY bit equal to one, saves the command and parameter values, then clears the BSY bit equal to zero.
7) As soon as the command is issued, the host may select the other device via DSEL and issue that device a command using the protocol for that command.
8) The host may remain with the current device selected and await an interrupt on the appropriate signal (i.e., INTRQ or INTRQ1).
9) If the current device supports command queuing, the host may issue another DMA data transfer command to that device using the appropriate command protocol as soon as BSY is cleared to zero.
10)


10) When the device is ready to transfer data it shall set DRQ equal to one, assert DMARQ, and then assertits interrupt signal. If an error has occured that aborts the transfer, Devcie 1 shall set CC equal to one and assert its interrupt signal.
11) If the host has the other device selected, it shall select the interrupting device via DSEL.
12) The host shall verify that DMARQ or DRQ is asserted.
13) If the device supports command queuing and the host has multiple commands outstanding tothe device, the host reads the Device/Head register to determine the command for which this interrupt was issued.
14) The host reads the Status register causing the device to negate its interrupt signal.
15) The host transfers the data.
16) The device may pause a transfer at any time by negating DMARQ and DRQ. In response to the negation of DMARQ, the host shall neagte DMACK. The host may pause a transfer at any time by negating DMACK.
DMACK negated
7), 8), or 9)
17)


17) When the data transfer has completed, the device shall negate DMARQ and DRQ and the host shall negate DMACK.
18) The host may select the other device via the DSEL signal and issue that device a command using the prescribed protocol for that command.
19) The host may remain with the current device selected and await an interrupt.
20) If the current device supports command queuing, the host may issue another DMA data transfer command to the device using the appropriate command protocol.
21) When the device is ready to report status it shall set CC equal to one and then assertits interrupt signal.
22) If the host has the other device selected, it shall select the interrupting device via DSEL.
23) The host shall read the Alternate Status register. The CC bit shall be equal to one.
24) If the device supports command queuing and the host has multiple commands outstanding to the device , the host reads the Device/Head register to determine the command for which this interrupt was issued.
25) The host shall read the error register for error information if ERR is set to one.
26) The host shall read the Status register. Upon completion of the Status register read the device shall set the CC bit equal to zero, negate its interrupt, and the command is complete.