TO: **John Lohmeyer, Chairman, X3T10 Committee (SCSI)**

From: Dennis Pak (408)974-4874
IEEE P1285 Liaison to X3T10

Date: April 17, 1998

Subject: P1285 Liaison Report for March 1995

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o Two interface levels: Beta & Gamma
- o Beta Level: 32-bit optimized, master/slave
- o Gamma Level: 64-bit optimized, master
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Self-synchronous data transfer
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

* The collaboration with P1596 SCI continues to finishing up. Another short co-located meeting will be held on March 24.

* Martin Freeman made a presentation on P1285 to the P1394 Trade Association General Meeting in January.

* The P1285 isochronous mover capability and rate-based control feature have been added.

* The P1285 working group voted to forward the P1285 document to the IEEE for balloting, subject to editorial changes.

* The document to be forwarded to the IEEE is currently undergoing editorial review.

Upcoming Events

Future meetings are scheduled as follows:

March 24 Co-located Meeting with IEEE 1596, Santa Clara University, Bannon Engineering Building, 12:15-1:30 PM.

March 29 Liaison Meeting with NSIC, Santa Clara University time TBD.

Meetings are usually scheduled from 2:00-5:00 PM. Comments and/or questions should be forwarded to Martin Freeman, IEEE P1285 Chair, @(415)354-0329. His e-mail address is martin@savant.PRPA.Philips.COM.