ATA-2 Forwarding Letter Ballot (X3T10/95-004) Results

Organization	Name	S	Yes	No	A	DNRB
3M Company	Mr. Alan R. Olson	P	1			
AMP, Inc.	Mr. Charles Brill	P	1			
AT&T		P				1
Adaptec, Inc.	Mr. Lawrence J. Lamers	A#	1			
Advanced Micro Devices	Mr. David Wang	P	1			
Amdahl Corp.	Mr. Edward Fong	P	1			
Amphenol Interconnect	Mr. Michael Wingard	A	1			
Ancot Corp.	Mr. Jan V. Dedek	P	1			
Apple Computer	Mr. Ron Roberts	A	1			
Burr-Brown Corp.	Mr. Dennis R. Haynes	P	1			
BusLogic	Mr. Clifford E. Strang Jr.	P	1			
CMD Technology	Mr. Edward Haske	P	1			
Ciprico Inc.	Mr. Gerry Johnsen	P	1			
Circuit Assembly Corp.	Mr. Ian Morrell	P	1			
Cirrus Logic Inc.		P				1*
Compaq Computer Corp.		P				1
Congruent Software, Inc.	Mr. Peter Johansson	P	1			
Conner Peripherals	Mr. Steven A. Anderson	A	1			
Dallas Semiconductor	Mr. Louis Grantham	P	1			
Digital Equipment Corp.	Mr. Charles Monia	P	1			
ENDL	Mr. I. Dal Allan	P	1			
Exabyte Corp.	Mr. Edward Lappin	P	1			
FSI Consulting Services	Mr. Gary R. Stephens	P	1			
Fujitsu Computer Products,Am	Mr. Robert Liu	P	1			
Future Domain Corp.		P				1
Hewlett Packard Co.	Mr. Jeffrey L. Williams	P	1			
Hitachi Micro Systems, Inc.	Mr. S. Nadershahi	P	1			
Honda Connectors	Mr. David McFadden	P	1			
IBM Corp.	Mr. George Penokie	P	1			
Interphase Corp.	Mr. David Lawson	P	1			
Iomega Corp.	Mr. Geoffrey Barton	P	1			
Linfinity Micro		P				1
Madison Cable Corp.	Mr. Robert Bellino	P	1			
Maxoptix Corp.	Ms. Donna Pope	P	1			
Maxtor Corp.	Mr. Pete McLean	P	1/C			
Methode Electronics, Inc.	Mr. Bob Masterson	P	1			
Molex Inc.	Mr. Joe Dambach	P	1			
NEC Technologies Inc.	Mr. Bruce Anderson	P	1			
National Semiconductor	Mr. Robbie Shergill	P	1			
Oak Technology, Inc.	Mr. Peter Brown	P	1			
QLogic Corp.		P				1
Quantum Corp.	Mr. James McGrath	P	1			
Seagate Technology	Mr. Gene Milligan	P	1			
Sequoia Advanced Tech., Inc.		P				1
Silicon Systems, Inc.	Mr. Stephen G. Finch	P	1			
Sony Corp. of America	Mr. Scott Smyers	P	1			
Storage Technology Corp.	Mr. Erich Oetting	P	1			
Sun Microsystems Computer Co		P				1*
SyQuest Technology Corp.	Mr. Patrick Mercer	P	1			
Tandem Computers	Mr. John Moy	P	1			
Thomas & Betts	Mr. Harvey Waltersdorf	P	1			
Trimm Industries		P				1
UNISYS Corporation	Mr. Peter Dougherty	P	1			
Unitrode Integrated Circuits	Mr. Paul D. Aloisi	P	1			
Western Digital Corporation	Mr. Tom Hanan	A#		1		
Woven Electronics	Mr. Doug Piper	P	1			
Zadian Technologies	Mr. Dennis P. Moore	P	1			
	Totals:		47	1	0	9

* NOTE: Late letter ballots were received from Joe Chen (Cirrus Logic) [No vote] and Bob Snively (Sun Microsystems)[Yes vote]. Joe's comments (95-163) were addressed by X3T10.

Comments Received:

From: Tom Hanan (714)932-7472
To: ATA; JOHN.LOHMEYER
Subject: ATA-2 Public Comments from Western Digital
Date: Thursday, March 02, 1995 10:44PM

During careful review of the ATA-2 document, and discussion with key non X3T10 IDE industry participants, the following editorial and technical issues were identified. I have separated the issues into editorial and technical to help identify issues which could be handled by the editor versus those which may require an agenda discussion at an upcoming X3T10 meeting.

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E D I T O R I A L C O M M E N T S
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1) Page 20, 4.3.I/O connector
The reference to figure 4 in the third paragraph should be changed to figure 3 to match the figure in this section.

2) Page 36, 6.2.12 Status Register
Change the DWF reference in the third paragraph of the BSY description to DF to match the table above.

3) Page 100,103,104,106
The diagrams on these pages are difficult to read and inconsistent with the style for the rest of the document. These diagrams should be reformatted as timing diagrams which are consistent in style with the rest of the document.

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T E C H N I C A L C O M M E N T S
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Because of the serious nature of the following technical issues Western Digital is forced to vote NO on the ballot to forward ATA-2 until these issues have been resolved. WD has received significant feedback from key non X3T10 participants which indicate that these issues will cause severe compatibility issues if not resolved before ATA-2 is forwarded.
In many cases the typical response of fixing the issue in ATA-3 is not acceptable because ATA-2 as written would then set a precedence for unreliable designs. Western Digital is committed to the concept of interoperability which has been the basis for IDE's popularity. Western Digital disagrees with the concept of allowing serious interoperability issues to be published only to be fixed in later publications.

Please add the following items to your agenda for ATA-2 public review technical comments.
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1) Page 21, Table 2, IOL(min)
Experiments and simulation by several independent developers, including WD's Physical Interface Group, indicate that the impedance of 12ma drivers is too low to match the impedance of the 18 inch ATA cable. 12ma drivers equate to an impedance of 35 ohms compared with the optimal impedance for the cable of 80-120 ohms. 4-6ma drivers have been proven to match the 80-120 ohm impedance of the ATA cable thereby minimizing settling times and the potential for data integrity issues across a wide range of configurations. This is a serious interoperability issue which affects the integrity of the standard we are about to publish.

The 12ma driver requirement is a hold over from the days when IDE controllers were forced to drive very large capacitive buses. Simulation has shown that 4ma drivers can reliably drive these Legacy configurations at Legacy timings because of improvements in the access times for VLSI devices compatible with ATA-2 timings.
Recommendation: "Change IOL(min) in table 2 from 12ma to 4ma for all signals except DASP and IOCS16. DASP and IOCS16 need the higher current to meet legacy timing and signal integrity issues.

2) Page 36, 6.2.12 Status Register
Add a note which recommends to BIOS developers that they take special precautions to address the issue of fast host systems reading the status register of older peripherals before the peripheral has finished updating the status register.

This has become a serious interoperability issue in environments where older ATA devices are mixed with newer ATA-2 devices. The problem is the result of the continuous performance improvements manufacturers have made to their CPU. Modern CPU bus managers can perform the status read following the last data transfer so quickly that older ATA devices cannot guarantee that they can provide valid status to the host system. Remember most ATA drivers are not designed to modify the timing of their low level ATA protocol drivers based on the speed of the processor.

3) Page 36, 6.2.12 Status Register
Remove the CORR bit from the third paragraph since the CORR bit is not allowed to change while BSY is 0.

4) Page 65, 8.10.17 Word 49: Capabilities
The section describing the function and use of Bit 13 is missing.

5) Page 71, 8.13 INITIALIZE DEVICE PARAMETERS For compatibility with existing products a note to BIOS developers should be added to this section. "Note: Some peripherals require this command prior to media access." Again this is a legacy issue where newer drivers designed using the ATA-2 standard would probably not achieve the existing level of interoperability without this note. Several BIOS and Driver developers have experienced compatibility issues related to this hidden ATA requirement.

6) Page 76, 8.18 READ LONG
For compatibility with existing products a note to Driver & BIOS developers should be added to this section.
"Note: Some older peripherals are not capable of delivering the 8bit ECC immediately after the word sector data. BIOS & Driver developers should take precautions to allow for this delay."
The arguments for this issue are identical to those in comment number 2 above.

7) Page 81, 8.23 SEEK
How do you know when this command is complete when we no longer have a definition for the DSC bit? This is a mandatory command!! Most BIOS and O/S drivers expect DSC to complete the seek command. Devices designed using the ATA-2 standard would have serious interoperability issues when used in pre ATA-2 configurations.

8) Page 95, 9.0 Protocol
The scenario in the third paragraph is a serious issue in PC based UNIX systems such as the SCO IDE drivers. A note should be added warning peripheral and UNIX developers that their drivers need to address this issue to achieve reliable operation.

9) Page 107, 9.7 Device 0 only configuration Item 1 of the Second method should be amended to include:
"Note: IDX is vendor specific and may change following reset resulting in other values for status besides 00h.

10) Page 115, 10.4.3 Multiword DMA Data Transfer The following note (3) should be added to tLr and tLw of figure 12:
"(3) tL is only a max when the peripheral cannot accept/provide the next data word."
This is an interoperability issue for controller hardware designed to work with both ATA and ATA-2 devices. Many pre ATA-2 devices used proprietary methods of DMA throttling which relied on their ability to guarantee that they could deliver the next word if the host missed the de-assertion of DREQ. DMA hardware designed without consideration for this issue would have serious interoperability issues with older ATA devices.

11) Page 119, A.5.2 Algorithm for Device 1
Item 9 should read the same as Item 9 on page 118.

12) Page 120, A.6.2 Algorithm for Device 1
Item 9 should read the same as page 97.

13) Page 121, A.7.2 Algorithm for Device 1
Item 8 should read the same as page 97.

14) Page 66, 8.10.22 Word 54 The following note should be added to this section:
"If the INITIALIZE DRIVE PARAMETERS command has not been issued to the device then the value of this word is vendor specific."
This is an ATA legacy device interoperability issue. BIOS and driver developers should be warned about this serious interoperability issue.

15) Page 66, 8.10.23 Word 55 The following note should be added to this section:

"If the INITIALIZE DRIVE PARAMETERS command has not been issued to the device then the value of this word is vendor specific."
See arguments for issue 14 above.

16) Page 66, 8.10.24 Word 56 The following note should be added to this section:
"If the INITIALIZE DRIVE PARAMETERS command has not been issued to the device then the value of this word is vendor specific."
See arguments for issue 14 above.

17) Page 130, D.
This entire section should be removed from ATA-2. The information contained within this section has caused more interoperability issues among driver and BIOS developers than it has resolved. Western Digital believes that this subject matter is already being addressed in the SYSTEMS working groups.

Yes Comment from Pete McLean of Maxtor Corp:

To: X3T10 Membership
From: Pete McLean - Maxtor Corporation
Subject: Comments on ATA Attachments Interface with Extensions (ATA-2) to accompany the positive vote on X3T10/95-004r0 letter ballot
Date: 6 February 1995

The following are believed to be only editorial in nature and should be easily resolved.

FORWARD - The reference to the AT Attachment Interface for Disk Drives should be changed from X3T9.2/791D to X3.221-1994.

1. SCOPE - The reference to the AT Attachment Interface for Disk Drives should be changed from X3T9.2/791D to X3.221-1994.

2. Normative references - The reference to the AT Attachment Interface for Disk Drives should be changed from X3T9.2/791D to X3.221-1994.

4. Interface Physical and Electrical Requirements - The reference to Annex C and Annex D should reference Annex B and Annex C.

4.3 I/O connector - In the third paragraph the reference to figure 4 should reference figure 3.

5.2.5 DD0-DD15 (Device Data) The reference to clause 8.23, Set Features should reference clause 8.24, Set Features.

6.1 Device Addressing Considerations - In the fourth paragraph, the reference to clause 6.2.8 should reference clause 6.2.7.

7.1 Reset response - In the third bullet in the first paragraph, the reference to clause 8.23 should reference clause 8.24.

8. Command Descriptions - In last note under Table 10, the reference to clause 6.2.10 should refer to clause 6.2.9.

8.8 EXECUTE DEVICE DIAGNOSTIC - In the DESCRIPTION section the reference to clauses 6.2.4 and 6.2.13 should reference clauses 6.2.8 and 6.2.12.

8.11 IDLE - the title of the table, Table 13 - Automatic Standby Timer Periods should be Table 13 - Automatic Idle Timer Periods.

8.24 SET FEATURES - In Table 14, the references to clause 8.24 are referring to the clause they are in. Should they be referring to something else?

9.5 Non-data commands - In the paragraph under the bullet list, the reference to clause 8.14 should reference clause 8.15 and the reference to clause 8.25 should reference clause 8.26.

A.4 Truth table - the title of the table, Table 14 - Reset Error register Values should be Table 16 - Reset Error register Values.