Date: Thu, 09 Feb 1995 16:07:56 +0000
From: "Hale Landis" <landis@sugs.tware.com>
To: "ATA Reflector" <ata@dt.wdc.com>
Subject: ATA-2 (ATA-3) Section 10.5
Extracted-To: ATA_Reflector

>From Hale to ATA Reflector.

Please refer to ATA-2 rev 2K...

In a recent discussion about the device 0/1 handshake on hard reset it was pointed out that ATA-2 Section 10.5 is confusing. Section 10.5 is the Power On and Hard Reset timing diagram. I have never liked this diagram -- it is too confusing to read.

One of the problems is that it tries to show what device 1 is doing with the DASP and PDIAG signals while at the same time showing what device 0 is also doing with these same signals. To be correct, the diagram should be split into two (or more) diagrams, one for device 0 only, one for both devices, etc.

The other problem, and the real reason I'm writing this note today, is that the table at the bottom of the diagram shows "tR Device 0 (max)" and "tR Device 1 (max)" but there is no tR shown for device 0 in the diagram. But if there was a tR for device 0 in the diagram, it would have to be explained as a "sampling time" and not a "max time period before device 0 asserts DASP" (device 0 doesn't assert DASP during a hard reset).

See the problem?

My current recommendation is: lets deleted the section 10.5 in ATA-3. Afterall, we have very good written description of this signal protocol in section 9.1 -- section 10.5 adds little (or nothing) to that description.

Now what should we do about ATA-2?

--
\\===============\\======================\\
\\ Hale Landis \\ 303-548-0567 \\
// Niwot, CO USA // landis@sugs.tware.com //
//===============//======================//