X3T10/95-152 R0

Quantum

Date: February 14, 1995
To: ATA/ATAPI Committee
From: Jim McGrath (408-894-4504)
Subject: Problems with System Implementation of Dual Ports

Background

One of the innovations in ATA technology that some suppliers are offering system customers is dual port - using the primary and secondary IDE disk controller addresses to allow the connection of up to 4 devices in a system, two per cable. This expands the number of devices (e.g. 2 WDDs, 1 CD-ROM, 1 tape drive), and in practice makes ATAPI CD-ROM usage possible.

Meanwhile, the electrical specifications for ATA are all based on the assumption of 1 or 2 devices per cable, and cables limited to 18 inches in length. Violating these constraints, either by adding more devices to the cable or lengthening the cable, would probably not work due to transmission line effects induced. While a host may be able to violate these restrictions under some circumstances, for a generic PC system using Fast IDE (mode 3 or mode 4) it is almost certain that the system would not function properly.

As conceived by the ATA and ATAPI standards, the new dual port feature works with these electrical limitations since two distinct cables are still used, each obeying the old electrical specifications.

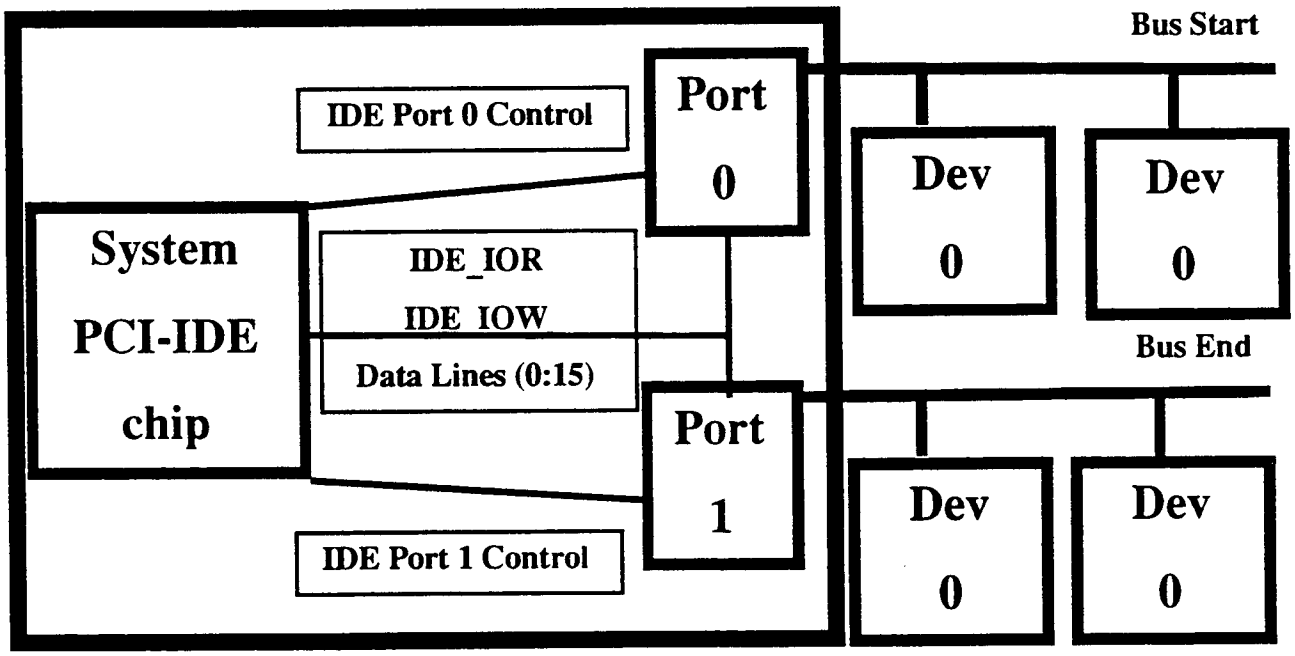
Problem

New PCI-IDE bridge chips and core system logic chip sets have begun to support both Fast IDE and multiple ports. However, many implementations grossly violate ATA and will result in major system integration problems. Even though devices may not be at fault, these bad system implementations will cost the industry time, effort, and possibly sales if our customer's shipments are delayed.

The problem is that, in the interest of saving pins for these system chips, the chip makers have often multiplexed the pins between the ports. Some control lines obviously cannot be multiplexed (e.g. IRQ). But clever design can allow some control lines to be multiplexed (e.g. IOR and IOW), and the data lines can always be logically multiplexed. Unfortunately, they cannot be physically multiplexed.

The restriction mentioned earlier on number of devices on a cable and length of a cable should really refer to "bus" not "cable." In the old, simple ATA world the bus was the cable (with some stubbing). But with 2 ports it is possible to create a system with 2 cables but one bus by multiplexing signals between the ports. Since the electrical restrictions apply to the bus, these systems will not work.

The figure below illustrates the problem. With IOR, IOW, and data multiplexed, the physical bus for these lines begins at the point marked "bus starts" and ends at the point marked "bus ends." It contains the two ATA cables and the traces on the system board connecting the cables to one another. Stubs are present at each device (4 stubs) and one in the middle of the bus to connect to the system chip. If the individual cables are 18 inches, then the total bus is 36-40 inches long (depending on the length of the traces on the system board) with 5 device loads. Under these circumstances the transmission line effects would generate errors for any device operating at Fast ATA speeds, and perhaps even at slower speeds.



Solution

This is one of the classic issues that is a system design problem impacting devices on the ATA cable. At a minimum people could spread knowledge of this issue, and pressure chip set vendors not to multiplex these lines. I believe notices in the ATA-3 standard (possibly an appendix) would help.

Alternatively, it is possible for system vendors to use external logic to fix this problem. In that case some guidance would be good, since I am sure any such design would otherwise be undesirable from a cost/complexity perspective.