Accredited Standards Committee*
X3, Information Processing Systems

Doc. No. X3T10/95-151r1
Date: February 17, 1995
Project:
Ref. Doc.:
Reply to: G. Milligan

To: Membership of X3T10

From: Lamers/Milligan

Subject: Minutes of X3T10 ATA Working Group - February 15-16, 1995

Agenda

1. Opening Remarks

Gene Milligan convened the meeting at 9:30 am. He thanked Jim McGrath of Quantum for hosting the meeting. He also requested that Larry Lamers take the minutes and thanked him for accepting the request.

As is customary, the people attending introduced themselves. A copy of the attendance list was circulated for attendance and corrections.

It was stated that the meeting had been authorized by X3T10 and would be conducted under the X3 rules. Ad hoc meetings take no final actions, but prepare recommendations for approval by the X3T10 task group. The voting rules for the meeting are those of the parent committee, X3T10. For the ad hoc, other than straw votes, the voting rules are: one vote per participating company.

The minutes of this meeting will be posted to the X3T10 BBS and the ATA Reflector and will be included in the next X3T10 committee mailing.

2. Attendance and Membership, Introductions

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or company to attend and to express their opinion on the subjects being discussed.

The following people attended the meeting.

NAME	ORGANIZATION	EMAIL
Mr. Lawrence J. Lamers	Adaptec, Inc.	ljlamers@aol.com
Mr. Ron Roberts	Apple Computer	rkroberts@aol.com
Mr. Kevin James	AMD	
Mr. Les Cline	Cirrus Logic	lesc@corp.cirrus.com
Mr. Joe Chen	Cirrus Logic Inc.	chen@cirrus.com
Mr. Marc Noblitt	Conner	marcnoblitt2conner.com
Mr. Hale Landis	Consultant	landis@sugs.tware.com
Mr. Robert Liu	Fujitsu Computer Products	
Mr. Jeff Epstein	Future Domain	jeffe@fdc.mhs.compuserve.com
Mr. Kevin Calvert	Future Domain	keving@fdc.mhs.compuserv.com
Mr. Dan Colegrove	IBM Corp.	colegrove@vnet.ibm.com
Mr. Lee Wilson	IBM PPS	
Mr. Duncan Penman	IIX	penman@netcom.com
Mr. Pete McLean	Maxtor Corp.	pete_mclean@maxtor.com
Mr. Peter Brown	Oak Technology, Inc.	brown@oaktech.com
Mr. Kevin Matsuda	Panasonic MKE	101175.176@compuserve.com
Mr. Curtis E. Stevens	Phoenix Technologies	curtis_stevens@bannet.ptltd.com
Mr. Farbod Falakfarsa	Quantum	
Mr. Jim McGrath	Quantum	jmcgrath@qntm.com
Mr. John Brooks	Quantum	jbrooks@qntm.com
Mr. Mark Evans	Quantum	mevans@qntm.com
Mr. Hank Davenport	Samsung	72102.1773@compuserve.com
Mr. Edward Hoskins	Seagate Technology	ed_hoskins@notes.seagate.com
Mr. Gene Milligan	Seagate Technology	gene_milligan@notes.seagate.com
Mr. Ron Werbow	Seagate Technology	ron_werbow@notes.seagate.com
Mr. John Masiewicz	Silicon Systems	john_masiewicz@notes.seagate.com
Mr. Patrick Mercer	SyQuest Technology	74754.1370@compuserve.com
Mr. Yas Hashimoto	Toshiba America	
Mr. K. T. Liang	Wearnes Technology	ktliang@wearnesj.com
Mr. Tom Hanan	Western Digital Corporation	hanan_t@a1.wdc.com
Mr. Virgil Wilkins	Western Digital Corporation	

3. Document Distribution

X3T10/95-145R0	Device 1 Only proposal	H. Landis
X3T10/95-152R0	Problems with System Implementation of Dual Ports	J. McGrath
X3T10/95-153R0	Enhanced Disk Drive Specification	C. Stevens
X3T10/95-154R0	Version Identification in ATA	H. Landis
X3T10/95-155R0	Comment on clause 10.5 of ATA-2	H. Landis
X3T10/95-156R0	BIOS Types, CHS Translation, LBA and other Good Stuff	H. Landis

4. Approval of Agenda

The agenda was approved as presented.

5. Review of Action Items

1) Gene Milligan to investigate the appropriateness of command queuing in the ATA-3 project proposal. Completed.
2) Larry Lamers to get document numbers for later inclusion in next minutes. Completed.
3) All participants are requested to post existing proposals for ATA-3 on the ATA reflector. Completed.
4) All participants to submit ATA-3 proposals for consideration in preliminary concept form by 11/10 and final form by January 12, 1995. Completed.

5) Gene Milligan to prepare and submit version indication proposal. Completed.
6) Devin Worrell to rename the A2 command to avoid the confusion with the DEV bit by 2/15/95.
7) Jeff Rabe to check to see if Intel will release for open control the definitions presently published in SFF 8037I and 80038I by 2/15/95. Carried over.
8) Devin Worrell to add appropriate specificity to the interaction of command overlap and power modes by 2/15/95. Carried over.
9) Devin Worrel to adjust the overlap and queuing proposal according to the results of this meeting and in particular to recast it in specification format suitable for detailed technical review and, if accepted, to have portions or the entire proposal integrated into the ATA Working Draft 2/15/95. Carried over.

6. Old Business

6.1 SFF Contributions

Tom Hanan stated that SFF-8029 revision 1.6 was submitted for the SFF mailing. The SFF-8020 revision 2 is in editorial review and will be sent to the SFF folks prior to the next meeting.

6.2 QIC Contributions

Gene stated there was no business.

6.3 ATA Software Programming Interface (ATASPI)

Kevin Calvert reported. Current version is 0.7 It is available on the Future Domain BBS (714-253-0432).

Issues have been raised regarding cross platform compatibility; advanced OS support; and multiple ASPI managers. There is a proposed modification to deal with advanced OS support under discussion. A proposal to modify the request flags to follow the latest ASPI specification. A proposal to modify the DSC bit meaning (however this bit is not defined in ATA-3) has been accepted by Future Domain. A proposal to change the Execute I/O request to ATAPI CDB. A proposal to support extended host adapter inquiry is being considered.

Kevin is working on a section regarding multiple managers and support for advanced OS.

6.4 ATAPI Plan and Schedule

Deferred due to uncertainty as to when SFF or others would make available an ATAPI proposal.

7. ATA-2 Items

Dan Colegrove stated that there is a problem with drives coming ready under the current system. The spec is up to 2 minutes but 30 seconds is more realistic, and is the maximum allowed in some IBM systems, to assertion of DRDY. He will develop a review comment on ATA-2.

8. ATA-3 Items

8.1 ATA-3 Command Overlap and Command Queuing Proposals

Quantum Issues - handling queuing with bridge chips with strong overlap can result in a problem when the host sends a command during a DMA data transfer because the CPU doesn't know it. The question is when and if an interrupt is generated by the drive bridge chip. John Brooks stated that a host should be able to send a command at any time including during a DMA transfer. This did raise the issue of fairness which needs to be addressed.
Tom Hanan pointed out that the current proposal from WD discriminates between a device being addressed vs. being selected. He further stated that this proposal does not allow for DMA data transfers to be interrupted by the host. A device could release DREQ and give up the bus; however there are timing issues. Hale Landis attempted to refocus the discussion on the basics of ATA signaling. This pointed out some fundamental timing issues that need to be addressed (e.g., DREQ has no restrictions on when it is reasserted during a data transfer).
Joe Chen raised an issue on the weak overlap regarding a race condition resulting in an interrupt glitch on the leading side and a missed interrupt on the trailing side. The group concluded that the scenario presented by Joe does not appear to be a problem. There is a window wherein if the driver does assure that the interrupt is deasserted that a clean edge may not occur. This is a system side issue and some guidance should be included in the standard.

John Masiewicz stated that a recent change in ATA-2 added a requirement that a host shall not drive chip select during DMA. This definitely affects strong overlap but does not appear to affect weak overlap.

Straw poll for level of capability for host system for first definition of strong overlap:

host interrupt of data transfer	7
without interrupt of data transfer	2

Straw poll for consideration of host hardware change:

allowed	9
disallowed	2

Straw poll for requiring a legacy mode for ATA-2 devices

unanimous

Straw poll for changes to host signals

allowed	poll abandoned
disallowed	poll abandoned

Tom Hanan - host viewpoint

a) weak

b) pio strong

c) dma strong with optional irq (performance limits on transfer length and number of interrupts)

d) dma strong without optional irq

Tom stated the host folks aim is to build drivers today that handles all four and wait for hardware on item d). Existing host side hardware could support items a), b), and c) today.

Jim McGrath does not believe item d) is possible since some systems do pre-fetch. The drive viewpoint would group items b), c), and d) since they change drive hardware.

The group's recommendation is that weak overlap will be considered for ATA-3. Proposals are requested.

Agreement on strong overlap was not reached at this meeting.

Curtis Stevens moved and Mark Noblitt seconded that strong overlap shall not be included in ATA-3. The motion passed unanimously.

8.2 PFA Reporting

The primary criticism came from Quantum regarding having the CORR bit set continuously. Some hardware implementations reset this bit on a command basis. A command execution polling is an alternative that Dan Colegrove will pursue.

8.3 Version Indication

Hale Landis presented a proposal for indicating the version level of a document that the device supports. The proposal has a major level and minor level to represent the project (ATA-2, ATA-3) and the document revision.

Tom Hanan requested that the word be recast as bit significant so that multiple levels of interface type could be represented. Hale stated he will generate a new proposal to reflect this.

8.4 Dynamic Power Selection

This proposal from Quantum and is aimed at flash memory cards. The sentiment was that it did not provide enough flexibility for rotating media, that have different power budgets if spun down vs spun up. Jim McGrath was not willing to expand the proposal but not against someone else offering a more comprehensive one.

Jim made one clarification. If the drive accepts the command, it agrees to not exceed the established power consumption (not just best effort) but may in the future abort some other command if that command would cause it to exceed the limit. Jim committed to include this clarification in the next revision.

8.5 Error Detection

There was no additional business on this item which is now closed for ATA-3.

8.6 IDENTIFY DRIVE BIOS Support

Curtis Stevens requested that consideration be deferred until he completes a more comprehensive proposal with similar objectives. His proposal should be available within 2-3 weeks. This proposal was deferred to ATA-4.

8.7 Working Draft Status

Pete McLean reported that he has a draft ATA-3 based on a cleaned up ATA-2 rev 2k and the five approved ATA-3 proposals. He asked whether weak overlap should be included in the draft before he releases the draft. The response was NO - that the current draft as is should be released. Proposals not approved by the ATA-3 working group are not be included in the draft document.

Straw poll - Those in favor of a statement of project goals to be included in Document Revision.
4 in favor; 7 opposed.

Pete McLean to release revision 0 incorporating the five accepted proposals prior to the next meeting.

9. Beyond ATA-3

9.1 Greater Than 16.6 MB

Joe Chen reported that his proposal is out there but has no comment. Curtis Stevens expressed a desire for 33 MB/sec as the next step not 22 MB/sec as in the proposal. There was sentiment expressed from drive folks to get a 25 MB/sec step. This would be adequate for drive bit density growth for the foreseeable future and should not require the electrical changes needed to achieve 33 MB/sec.

9.2 28 bits

Curtis Stevens reported a potential problem with size inflation of disk drives. The maximum sector addressing is currently 28 bits allowing for 137 GB disk drives. This is a long term issue but needs a long term solution and needs some consideration for ATA-4.

10. New Business

10.1 Multiple Connector ATA Implementations

There are implementations of PCI-IDE bridge chips that implement two ports with separate signals for control but bussed signals for the data including in some cases the OR/IOW signals. Bussing signals in a 'Y' arrangement where the cable length violates the ATA-2 standard. John Masiewicz raised this issue as a warning to the industry.

Hale Landis pointed out that even if you solve the electrical problem, multi-threaded I/O for OS/2, Win95, still will not work correctly if there are multiple devices on each logical cable (>2 on the combined cable). Others held that this aspect was dealt with by the bridge including all the facilities of two host adapters save the provision for driving two completely separate physical cables.

Larry Lamers pointed out that the many chip & board manufacturers are unsympathetic since they don’t violate the specification. They are providing a low-cost solution demanded by the marketplace. It’s the user who violates the specification when he attaches the cables.

The current draft standard clearly states that exceeding the 18-inch bus length is prohibited. The issue is education - making system integrators and end users aware of the pitfalls.

Manufactures are requested to work on applications notes and white papers to be submitted to SFF for publication.

10.2 Enhanced Disk Drive Specification

Curtis Stevens presented the current version of the Phoenix specification. He called attention to the sections on 528 MB and translations for review. There also is a stab at a real mode hardware interface to set up things like pre-fetch.

Hale Landis mentioned that he is developing a BIOS types document to help people understand what works with what.

10.3 ATA Lite

Hale Landis reviewed the outline he had posted on the reflector. There was skepticism on whether the changes he had proposed so far would offer any savings over the standard ATA.

10.4 DASP Timing Diagram

Hale Landis reported that there are questions regarding the polling time for DASP. The polling regarding DASP following hard reset is worded consistently but the diagram is misleading and should be deleted.

Curtis Stevens moved and Duncan Penman seconded to remove the misleading diagram. Withdrawn to allow further consideration.

This will be considered at the next meeting.

10.5 CS0, CS1

John Masiewicz reported that CS0 and CS1 are required to be not driven in ATA-2 during DMA. This statement affects host silicon making them illegal. He suggested adding a statement to ATA-2 stating that this was not a previous requirement and will be removed in ATA-3.

Hale Landis volunteered to write a proposal that removes the wording.

10.6 Set Multiple Elimination

Hale Landis will develop a proposal to remove the set multiple function.

11. Call for Patents

Gene Milligan requested that anyone aware of any patents required for the proposals be disclosed early in accordance with the ANSI patent policy.

Prior minutes have reported that: “The Secure Mode proposal involves patents pointed out by Pete McLean and he stated that a letter has been submitted by Maxtor. He also mentioned an IBM patent and Dan Colegrove noted that document 94-125 contains the letter regarding the ANSI patent policy.”

12. Action Items

10) Gene Milligan will request a study effort for the items not included into ATA-3.
11) Gene Milligan to get document for device one support.
12) Gene Milligan to conduct vote on CS0, CS issue.
13) Gene Milligan to add DASP and drive ready time-out to March agenda.
14) Larry Lamers to find a contact within Adaptec on ASPI for chairman.

13. Meeting Schedule

March 8-9, 1995 in Orange County hosted by Q Logic.
April 12-13, 1995 probably in Longmont, CO.
Jun 21-22, 1995

14. Adjournment

The meeting adjourned upon completion of business on February 16, 1995.