NCR Microelectronic Products Division

Date: January 25, 1995
To: X3T10 Membership
From: John Lohmeyer
Subject: Minimum Negation Current Issue with Fast-20

After reading the SCSI Reflector messages on this topic and discussing the topic with our chip designers, I'd like to propose that section 6.1.2 be modified as shown in the document. It would replace items c), d), and e) from the output characteristics list with a new item c):

"c) The output sourcing characteristics (signal negated) shall be constrained to operate in the non-shaded areas of figure 1."

Figure 1 is new. It has the same characteristics for the old items c) and d) and reduces the drive requirements from the old item e) to a linear function going from points (0 V, 22 mA to 2 V, 0 mA).

All other portions of the proposed section 6.1.2 are not changed from Fast-20 Rev 3. Of course, if this proposal is adopted, the other figures in Fast-20 would have to be renumbered.

While X3T10 may treat this proposal as an advanced copy of a public review comment against Fast-20, I would prefer that the issue be dealt with prior to public review.

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6.1.2 Single-ended output characteristics

Single-ended signals shall use active-negation drivers. Active-negation drivers have three states: asserted, negated, and high-impedance. Each signal sourced by an SCSI device shall have the following output characteristics when measured at the SCSI device's connector:

a) VOL (low-level output voltage) = 0,0 to 0,5 V d.c. at IOL = 48 mA (signal asserted);
b) V_{OH} (high-level output voltage) = 2,5 to 3,7 V d.c. (signal negated);
c) The output sourcing characteristics (signal negated) shall be constrained to operate in the non-shaded areas of figure 1.

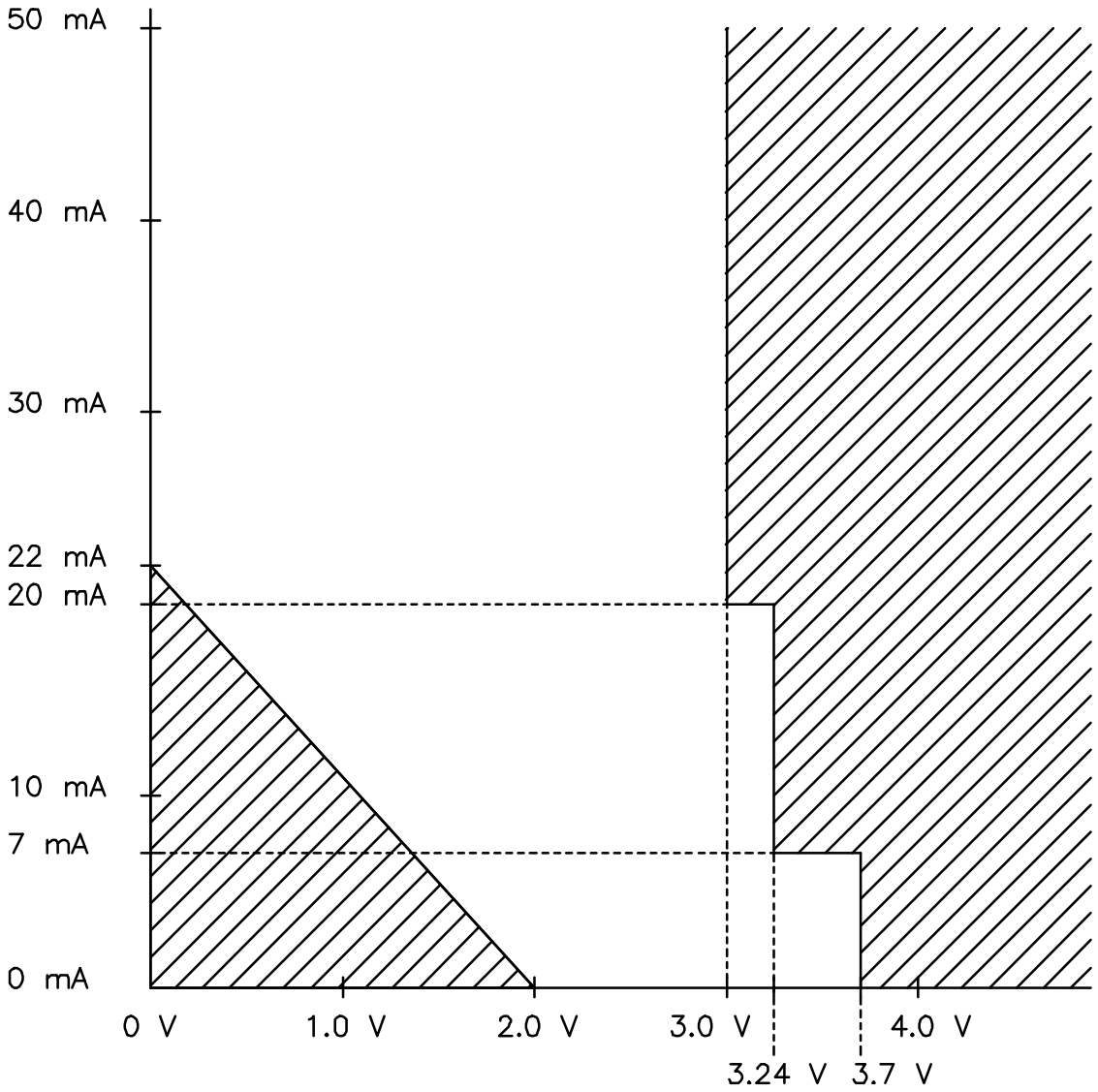

Figure 1 -- Active Negation Current vs. Voltage

All single-ended drivers shall maintain the high-impedance state during power-on and power-off cycles.

SCSI devices should meet the following specifications for all signals when measured on the test circuit shown in figure 2 with a load capacitor (C_L) of 15 pF +/- 5%:

a) trise (rise rate) = 520 mv per ns maximum (0,7 V d.c. to 2,3 V d.c.);
b) tfall (fall rate) = 520 mv per ns maximum (2,3 V d.c. to 0,7 V d.c.).

All other output timing specifications shall be measured with the test circuit shown in figure 2 with a load capacitor (C_L) of 200 pF +/- 5%.

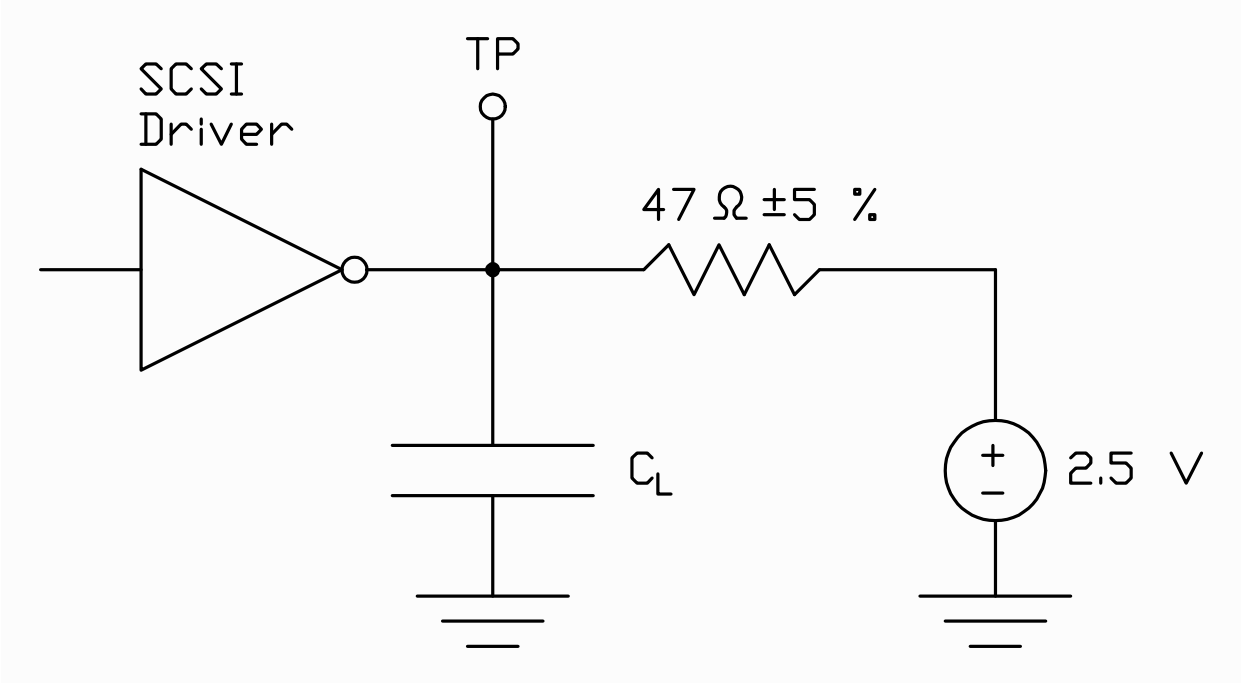

Figure 2 - Single-ended test circuit