

TO: John Lohmeyer, Chairman, X3T10 Committee (SCSI)

From: Dennis Pak (408)974-4874
IEEE P1285 Liaison to X3T10/DADI

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Subject: P1285 Liaison Report for January 1995

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o Two interface levels: Beta & Gamma
- o Beta Level: 32-bit optimized, master/slave
- o Gamma Level: 64-bit optimized, master
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Self-synchronous data transfer
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

* The collaboration with P1596 SCI is finishing up. Another co-located meeting will be held on January 12.

* The beta level data structures have been updated to allow for both 32-bit and 64-bit operation.

* A new P1285 document update is imminent. The beta level and gamma level portions of the document have already been updated.

* New features include:

- Mover capability: the reporter
- Setup command for 64-bit addressing
- Event handling support

- Scatter/Gather for beta level
- Command pre-fetching support for the beta level

Upcoming Events

Future meetings are scheduled as follows:

January 12 Co-located Meeting with IEEE 1596, Santa Clara University,
Bannon Engineering Building

Meetings are usually scheduled from 2:00-5:00 PM. Comments and/or questions should be forwarded to Martin Freeman, IEEE P1285 Chair, @(415)354-0329. His e-mail address is martin@savant.PRPA.Philips.COM.