To: X3T10 ATA Working Group

From: Steve Finch
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Date: January 5, 1995

Subject: Annex F

In the last month, there has been a lot of email discussion on the contents of Annex F. This document is an attempt to focus the discussion and come to a resolution.

I think the issue is not a single issue, but a number of related issues.

1. Do we need to address this before requesting the document to be forwarded. If the answer is no, then we can “fix it” when we resolve letter ballets.
<I personally would like to see it fixed now.>

2. Does this information belong in the ATA-2 standard. If the answer is no, we can delete Annex F and be done.
<I think it provides useful information for new users of ATA and, because it is an informative Annex, does not distract from the standard.>

3. How much information do we want in the document? The options are to define this information for one, two, three, four or ?? ports. A secondary question is: with or without the interrupt vectors.
<I believe the original Annex should have had interrupt usage information and this information should be added.>
<If we can agree on ports 3 and 4 definitions, I believe this would help the industry as a whole, but I also understand that this is “allocating” a fixed resource and could become a major issue in the industry. My net result is: I’ll agree with the majority...>

4. Is this an informative Annex or ??
<I believe this Annex is and always will be informative, as ATA-2 can be and is used in non-x86 systems.>

5. Should we add operating system support? With revisions numbers?
<I believe that adding this information is in appropriate to a device interface.>

In the following pages, I have tried to come up with what I believe are the set of most likely options. I suggest that we choose the best fit and then, if necessary, modify it to get the desired results.

I believe I can easily incorporate any changes into the document today.

<Option 1: Leave it alone>
<DIRECTLY FROM 0948DR2J>

Annex F. IBM PC AT(tm) Interface Addresses (informative)

In the IBM PC AT(tm), an ATA interface utilizes two address select lines (CS0- and CS1-) which are the result of an address decode on the personal computer's main board or on an adapter board which is installed in the personal computer. Some PCs utilize more than one ATA interface. In these systems each interface needs a separate set of address decodes. The BIOS (Basic Input/Output System) and operating systems installed within these computers have established defacto standards for the I/O addresses used to address the ATA interfaces. While the number of ATA interfaces supported by a particular system implementation vary, the following table lists the addresses typically used.

This information is provided for information only. There is no requirement that an implementation utilize these addresses.

Interface Number	CS0- Decode	CS1- Decode
1	01Fxh	03Fxh
2	017xh	037xh
3	00Fxh	02Fxh
4	007xh	027xh

Table 21 - Typical PC Interface Address Assignments

<Option 2: Only incorporate 2 port definitions as these can be agreed upon and add interrupt numbers.>

Annex F. IBM PC AT(tm) Interface Addresses and Interrupts (informative)

In the IBM PC AT(tm), an ATA interface utilizes two address select lines (CS0- and CS1-) which are the result of an address decode on the personal computer's main board or on an adapter board which is installed in the personal computer. Some PCs utilize more than one ATA interface. In these systems each interface needs a separate set of address decodes. The BIOS (Basic Input/Output System) and operating systems installed within these computers have established defacto standards for the I/O addresses used to address the ATA interfaces. While the number of ATA interfaces supported by a particular system implementation vary, the following table lists the addresses typically used.

This information is provided for information only. There is no requirement that an implementation utilize these addresses.

Interface Number	CS0- Decode	CS1- Decode	IRQ Number
1	01F0h-01F7h	03F6h-03F7h	14
2	0170h-0177h	0376h-0377h	15 or 10

Table 21 - Typical PC Interface Address Assignments

<Option 3A: Fix all 4 port definitions and add interrupts. Leave a little flexibility in the interrupts.>

Annex F. IBM PC AT(tm) Interface Addresses and Interrupts (informative)

In the IBM PC AT(tm), an ATA interface utilizes two address select lines (CS0- and CS1-) which are the result of an address decode on the personal computer's main board or on an adapter board which is installed in the personal computer. Some PCs utilize more than one ATA interface. In these systems each interface needs a separate set of address decodes. The BIOS (Basic Input/Output System) and operating systems installed within these computers have established defacto standards for the I/O addresses used to address the ATA interfaces. While the number of ATA interfaces supported by a particular system implementation vary, the following table lists the addresses typically used.

This information is provided for information only. There is no requirement that an implementation utilize these addresses.

Interface Number	CS0- Decode	CS1- Decode	IRQ Number
1	01F0h-01F7h	03F6h-03F7h	14
2	0170h-0177h	0376h-0377h	15 or 10
3	01E8h-01EFh	03EEh-03EFh	12 or 11
4	0168h-016Fh	036Eh-036Fh	10 or 9

Table 21 - Typical PC Interface Address Assignments

<Option 3B: Fix all 4 port definitions and add interrupts. Make interrupts fixed.>

Annex F. IBM PC AT(tm) Interface Addresses and Interrupts (informative)

In the IBM PC AT(tm), an ATA interface utilizes two address select lines (CS0- and CS1-) which are the result of an address decode on the personal computer's main board or on an adapter board which is installed in the personal computer. Some PCs utilize more than one ATA interface. In these systems each interface needs a separate set of address decodes. The BIOS (Basic Input/Output System) and operating systems installed within these computers have established defacto standards for the I/O addresses used to address the ATA interfaces. While the number of ATA interfaces supported by a particular system implementation vary, the following table lists the addresses typically used.

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3	01E8h-01EFh	03EEh-03EFh	11
4	0168h-016Fh	036Eh-036Fh	10

Table 21 - Typical PC Interface Address Assignments