November 9, 1994

TO: ATA Committee
FROM: Intel/PCD(PCI Components Division)
CONCERNING: ATA-3 Command Overlap and Command Queuing Proposal

ATA has flourished in the mainstream, high volume segment of the PC market due its price/performance advantage over competing interface standards. Intel/PCD is concerned that some of the recently proposed extensions in the form of draft ATA3 specifications may erode this price performance advantage. The following briefly summarizes our current position on these proposals. Our objective is to see the price/performance of the ATA standard maintained and enhanced.

For the following discussion, "Command Overlapping" refers to the ability to issue a second command (to a second device) on an IDE channel, before the first command (to the first device) completes. The seek times of the two devices are thus overlapped, and the faster device (ie, HDD, with seek times of a few ms) need not wait for the slower device (ie CD ROM, with seek times of hundreds of ms) to complete its command. The term "Command Queueing" refers to the ability of a single ATA device to accept multiple commands (up to a defined queue depth) before completing the first. Commmands may be completed out of order in some queueing proposals.

Command Overlapping appears to meet the objective of maintaining the price performance advantage of ATA. The additional host and drive controller complexity seems manageable while the potential improvement in performance (with a muti-tasking OS) and reduction in cost (hard drive and ATAPI CD-ROM drive on one IDE channel) is attractive. On the other hand, Command Queueing adds complexity without demonstrated benefit to the end user in a standalone desktop or client environment, by far the volume segment. This added complexity burdens the computation and firmware requirements internal to the drive, and also mandates additional functionality in the host adapter, especially those which provide a bus master type interface. This additional complexity is likely to result in higher cost. Additionally, ease of use issues may plague the introduction of complex new technology which requires co-ordination of the BIOS, OS driver, ATA peripheral and host adapter vendors.

Intel would like to see CPU cycles being used to increase the functionality and performance of the system as visible by the end user. To that end, we have been successful in promoting a bus mastering standard for ATA peripherals. Intel/PCD would like to participate in the definition of extensions to the ATA spec, and maintain momentum of the bus mastering spec as a standard. At this time we feel Command Overlap is a needed capability and would like to work with others on the commitee to work out the technical issues. If the ATA committee feels that it is imparative to define a Command Queuing it should be defined as an optional superset of Command Overlapping.