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To: John Lohmeyer, Chairman, X3T10 X3T10/94-217r0

Copy: SCSI-3 WG and interested parties

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Subj: Proposed Implementor's Note for Device Capacitance and Spacing for Fast-20 SCSI

The SCSI bus is a distributed parameter circuit whose electrical characteristics and responses are primarily defined by the distributed inductance and capacitance along the physical media. The media is defined here as the interconnecting cable(s) or conducting paths, connectors, terminators, and SCSI devices added along the bus. The following analysis derives a guideline for the amount of capacitance (and its spacing) that can be added to the Single-ended Fast-20 SCSI bus.

To a good approximation, the characteristic transmission line impedance seen into any cut point in the unloaded SCSI bus is defined by $Z = \sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus, in the form of devices and their interconnection, the bus impedance is lowered and can be expressed by $Z' = \sqrt{L/(C + C')}$, where C' is the added capacitance per unit length. When capacitance is added to the bus by devices, an impedance mismatch occurs and when a signal wave arrives at this mismatch in impedance, an attenuation (or amplification) of the signal will occur. The magnitude of the attenuation will depend upon the ratio of the mismatched impedance or $A = Z'/Z$, where Z' is the load impedance and Z is the source impedance.

Substituting the equations for Z' and Z and reducing,

1) $$A = Z'/Z = \frac{\sqrt{L/(C + C')}}{\sqrt{L/C}} = \sqrt{\frac{1}{(1 + C'/C)}}.$$

We now have a relationship for the attenuation of the signal voltage at an impedance mismatch due to load capacitance distributed on the SCSI bus. Next, a rule for the ratio of Z' to Z will be derived.

With fast transfer rates and electrically long[1] media, it becomes essential to achieve a valid input voltage level on the **first** signal transition from an output driver anywhere on the bus. This is called incident-wave switching. If incident-wave conditions are not achieved, reflected-wave switching must be used. Reflected-wave switching depends upon reflected energy occurring some time after the first transition arrives to achieve a valid logic voltage level. In the Fast-20 SCSI environment, the valid low-level input voltage threshold has been raised and the high-level input voltage threshold has been lowered to allow incident-wave switching with some inevitable impedance mismatching and signal attenuation along the media.

The signal voltage at an impedance mismatch is $V_{L1} = V_{L0} + V_{J1} + V_{R1}$, where V_{L0} is the initial voltage, V_{J1} is the input signal voltage, and V_{R1} is the reflected voltage. The voltage reflected back from the mismatch is $V_{R1} = \rho_L \times V_{J1}$

[1] *Electrically long* is defined here as $\tau > \frac{t_{10-90\%}}{3}$, where τ is the one-way time delay across the bus and $t_{10\text{-}90\%}$ is the 10% to 90% transition time of the fastest driver output signal.

where, $\rho_L = \frac{Z' - Z}{Z' + Z}$ and is the coefficient of reflection commonly use in transmission line analysis. The voltage equation can now be written as $V_{L1} = V_{L0} + V_{J1} + \rho_L \times V_{J1}$.

When a SCSI signal is asserted, the V_{L0} can be at a maximum of 3.7 V and go to 0 V (for a perfect driver) giving a V_{J1} of -3.7 V and the signal voltage must go below the minimum receiver input voltage threshold of 1 V. In equation form, $1 > 3.7 + (-3.7) + \rho_L \times (-3.7)$ $\rho_L > \frac{1 - 3.7 + 3.7}{-3.7} = -0.27$. The negative value means that no more than 27% of the input signal voltage can be reflected **back** towards the source or the minimum assertion level will not be achieved by the incident wave[2].

Now, to relate this to Z'/Z and using equation 1) for C'/C,

2)
$$\rho_L = \frac{Z' - Z}{Z' + Z} > -0.27$$
$$Z' - Z > -0.27(Z' + Z)$$
$$Z'(1 + 0.27) > Z(1 - 0.27)$$
$$\frac{Z'}{Z} > \frac{0.73}{1.27} = 0.57$$

and

$$0.57 < \sqrt{\frac{1}{(1 + \frac{C'}{C})}}$$
$$\frac{1}{0.57^2} - 1 > \frac{C'}{C}$$
$$\frac{C'}{C} < 2.08$$

We can now say that capacitance should not be added at more than twice the bus distributed capacitance for incident wave switching. For example, a cabled bus with L = 295 nH/m (90 nH/ft) and C = 41 pF/m (12.5 pF/ft) and Z = 85Ω, the guideline becomes to add no more than 85 pF/m (26 pF/ft) anywhere along the bus. This guideline can be met by 25 pF loads spaced 0.3 m (1 ft) from each other, 50 pF spaced 0.6 m (2 ft) apart, or 12.5 pF spaced 0.15 m (0.5 ft) apart. This relationship is shown graphically in figure 1.

[2]A similar analysis can be used for the negation case of 0 V to 2.8 V ([48 mA + 22 mA] x 40Ω) and an input voltage threshold of 1.9 V for a minimum reflection coefficient of -0.32. This leaves assertion as the most restrictive case.

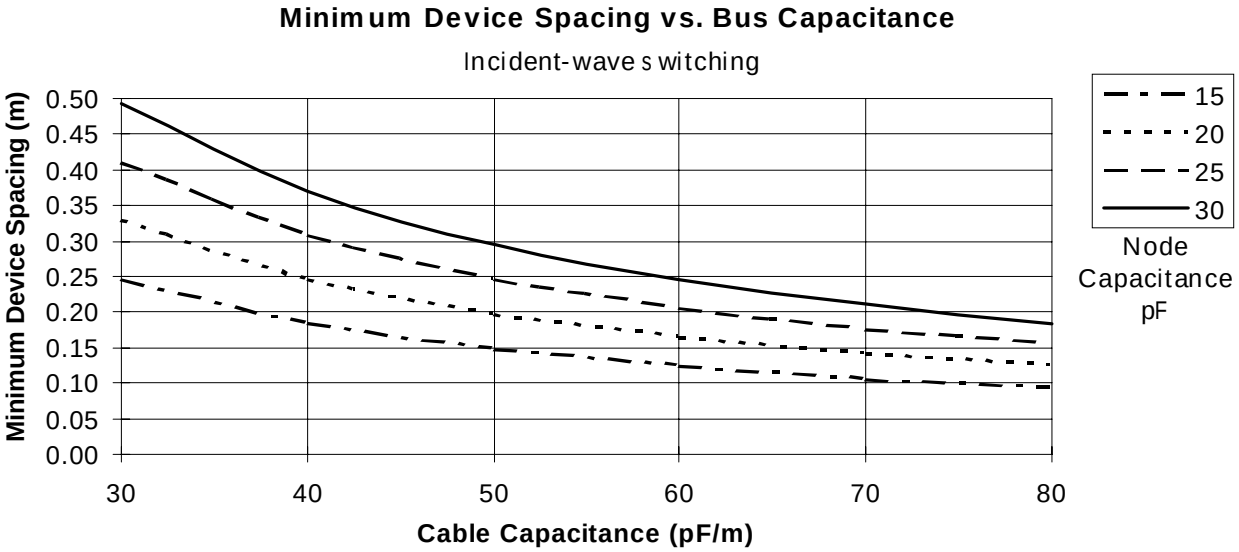

Figure 1. Minimum device spacing versus bus and device capacitance.