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To: ATA Working Group, X3T10

From: Steve Finch, Silicon Systems Inc.

Subject: Clarification/Expansion to Table 7 of ATA-2 (Address decoding)

I believe we are missing a some necessary information in the ATA-2 proposed standard. The type of information I'm referring to involves the response of the device to various combinations of signals on the ATA bus. While this information is "obvious" for most of us, I have received a number of questions on how to handle certain conditions. I think the following table provides this missing information, and I propose that we either replace Table 7 in section 6.2, or add this table in the same section.

I have one question whose answer may change the table. When DMARQ is active and DMACK is active, the timing diagrams do not specify the state of the address lines and, more specifically, the chip select lines (CS0- and CS1-). Is it possible that, when a DMA transfer is in progress, that the chip select lines may be active (e.g., due to floating ISA bus signals after the previous register access)? The proposed table currently states that when a DMA is active, i.e. DMARQ and DMACK are both active, that the chip selects must not be active. Perhaps the answer should be that these signals are ignored.

The table does not address the issue of the DEV bit (device select). The following text addresses this issue. The best location of this text is probably just before the table.

"The ATA interface consists of a single host and one or two devices. Operation of a device on the ATA interface is, in some cases, dependent upon configuration of the interface and upon whether the device is selected. Via the configuration process defined in Clause 4.1, a device is assigned a device number of either 0 or 1. A device is selected when it is configured as Device 0 and the DEV bit is equal to zero, or when it is configured as Device 1 and the DEV bit is equal to one.

All devices attached to the ATA interface, whether selected or not, shall accept PIO write operations as described in Table x, except that a device may ignore writes to the Data register if it is not currently selected.

With the exception of a single device on the ATA interface which is configured as Device 0, a device shall respond to PIO read operations only if it is currently selected. A device configured as Device 0 that has determined via DASP- signal during the power on and/or RESET protocol that it is a single device on the ATA interface, shall also respond to a PIO read of the Status register when Device 1 is selected and the recommended response is a status value of all zeros.

A device may drive the DMARQ only if it is selected. A device shall only honor DMACK if it is currently driving DMARQ.

The host shall not write to any task file register while the BSY bit of the currently selected device, as reflected in the Status or Alternate Status registers, is equal to one."

DMARQ	DMACK-	CS1-	CS0-	A2	A1	A0	BSY	DRQ	DEV	IOR-	IOW-	Result
x	x	0	0	x	x	x	x	x	x	0	x	Illegal/Undefined
x	x	0	0	x	x	x	x	x	x	x	0	Illegal/Undefined
x	x	x	x	x	x	x	x	x	x	0	0	Illegal/Undefined
1	0	0	x	x	x	x	x	x	x	0	x	Illegal/Undefined
1	0	0	x	x	x	x	x	x	x	x	0	Illegal/Undefined
1	0	x	0	x	x	x	x	x	x	0	x	Illegal/Undefined
1	0	x	0	x	x	x	x	x	x	x	0	Illegal/Undefined
0	x	1	1	x	x	x	x	x	x	x	x	None
1	1	1	1	x	x	x	x	x	x	x	x	None
x	x	x	x	x	x	x	x	x	x	1	1	None
x	x	x	x	x	x	x	x	x	x	1	0	None (Writes are ↑ edge triggered)
1	0											DMA Cycle
1	0	1	1	x	x	x	1	x	x	0	1	Note 8
1	0	1	1	x	x	x	1	x	x	1	↑	Note 8
1	0	1	1	x	x	x	0	0	x	0	1	Note 9
1	0	1	1	x	x	x	0	0	x	1	↑	Note 9
1	0	1	1	x	x	x	0	1	x	0	1	Transfer to Data register (Note 4)
1	0	1	1	x	x	x	0	1	x	1	↑	Transfer from Data register (Note 5)
		0	1									Control Block Registers
0	x	0	1	0	x	x	x	x	x	x	x	None
1	1	0	1	0	x	x	x	x	x	x	x	None
0	x	0	1	1	0	x	x	x	x	x	x	None
1	1	0	1	1	0	x	x	x	x	x	x	None
0	x	0	1	1	1	0	x	x	x	0	1	Read Alternate Status register
1	1	0	1	1	1	0	x	x	x	0	1	Read Alternate Status register
0	x	0	1	1	1	0	x	x	x	1	↑	Write to Device Control register
1	1	0	1	1	1	0	x	x	x	1	↑	Write to Device Control register
0	x	0	1	1	1	1	x	x	x	0	1	(Note 1)
1	1	0	1	1	1	1	x	x	x	0	1	(Note 1)
0	x	0	1	1	1	1	x	x	x	1	↑	None
1	1	0	1	1	1	1	x	x	x	1	↑	None

DMARQ	DMACK-	CS1-	CS0-	A2	A1	A0	BSY	DRQ	DEV	IOR-	IOW-	Result
		1	0									Command Block Registers
0	x	1	0	0	x	x	1	x	x	0	1	Read of Alternate Status register
1	1	1	0	0	x	x	1	x	x	0	1	Read of Alternate Status register
0	x	1	0	x	0	x	1	x	x	0	1	Read of Alternate Status register
1	1	1	0	x	0	x	1	x	x	0	1	Read of Alternate Status register
0	x	1	0	x	x	0	1	x	x	0	1	Read of Alternate Status register
1	1	1	0	x	x	0	1	x	x	0	1	Read of Alternate Status register
0	x	1	0	x	x	x	1	x	x	1	↑	None (Note 2)
1	1	1	0	x	x	x	1	x	x	1	↑	None (Note 2)
0	x	1	0	0	0	0	0	0	x	0	1	Note 3
1	1	1	0	0	0	0	0	0	x	0	1	Note 3
0	x	1	0	0	0	0	0	0	x	1	↑	Note 3
1	1	1	0	0	0	0	0	0	x	1	↑	Note 3
0	x	1	0	0	0	0	0	1	x	0	1	Read of Data register (Note 4)
1	1	1	0	0	0	0	0	1	x	0	1	Read of Data register (Note 4)
0	x	1	0	0	0	0	0	1	x	1	↑	Write of Data register (Note 5)
1	1	1	0	0	0	0	0	1	x	1	↑	Write of Data register (Note 5)

DMARQ	DMACK-	CS1-	CS0-	A2	A1	A0	BSY	DRQ	DEV	IOR-	IOW-	Result
		1	0									Command Block Registers (continued)
0	x	1	0	0	0	1	0	x	x	0	1	Read of Error register
1	1	1	0	0	0	1	0	x	x	0	1	Read of Error register
0	x	1	0	0	0	1	0	x	x	1	↑	Write of Feature register
1	1	1	0	0	0	1	0	x	x	1	↑	Write of Feature register
0	x	1	0	0	1	0	0	x	x	0	1	Read of Sector Count register
1	1	1	0	0	1	0	0	x	x	0	1	Read of Sector Count register
0	x	1	0	0	1	0	0	x	x	1	↑	Write of Sector Count register
1	1	1	0	0	1	0	0	x	x	1	↑	Write of Sector Count register
0	x	1	0	0	1	1	0	x	x	0	1	Read of Sector Number register
1	1	1	0	0	1	1	0	x	x	0	1	Read of Sector Number register
0	x	1	0	0	1	1	0	x	x	1	↑	Write of Sector Number register
1	1	1	0	0	1	1	0	x	x	1	↑	Write of Sector Number register
0	x	1	0	1	0	0	0	x	x	0	1	Read of Cylinder Low register
1	1	1	0	1	0	0	0	x	x	0	1	Read of Cylinder Low register
0	x	1	0	1	0	0	0	x	x	1	↑	Write of Cylinder Low register
1	1	1	0	1	0	0	0	x	x	1	↑	Write of Cylinder Low register
0	x	1	0	1	0	1	0	x	x	0	1	Read of Cylinder High register
1	1	1	0	1	0	1	0	x	x	0	1	Read of Cylinder High register
0	x	1	0	1	0	1	0	x	x	1	↑	Write of Cylinder High register
1	1	1	0	1	0	1	0	x	x	1	↑	Write of Cylinder High register
0	x	1	0	1	1	0	0	x	x	0	1	Read of Device/Head register
1	1	1	0	1	1	0	0	x	x	0	1	Read of Device/Head register
0	x	1	0	1	1	0	0	x	x	1	↑	Write of Device/Head register
1	1	1	0	1	1	0	0	x	x	1	↑	Write of Device/Head register
0	x	1	0	1	1	1	x	x	x	0	1	Read of Status register (Note 6)
1	1	1	0	1	1	1	x	x	x	0	1	Read of Status register (Note 6)
0	x	1	0	1	1	1	0	x	x	1	↑	Write of Command register
1	1	1	0	1	1	1	0	x	x	1	↑	Write of Command register
									0			Note 7
									1			Note 7

Note 1: This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall be sure not to drive the DD7 signal to prevent possible conflict with floppy disk implementations.

Note 2: By definition, writing to any Command Block Register when BSY is set is not valid and shall be ignored by the device. However, BSY can be reset by the device at any time and, therefore, the timing of the write by the host when the host believes BSY is set may actually occur after the device has reset BSY. In this case, the host can not determine if the write was performed or not. Writing to any Command Block Register when BSY is set should not be attempted.

Note 3: Results of reading or writing the Data Register when DRQ is not set is undefined.

Note 4: This assumes that the device expects that the data transfer is toward the host. If the device expects the data transfer is from the host (write type of operation), then the results are undefined and subsequent data transfers for the current command are indeterminate.

Note 5: This assumes that the device expects that the data transfer is from the host. If the device expects the data transfer is toward the host (read type of operation), then the results are undefined and subsequent data transfers for the current command are indeterminate.

Note 6: Read of the Status register is not dependent on the BSY bit. Reading of the Status register resets the internal interrupt condition as held by the device which is currently selected. The generation of INTRQ is based on the internal interrupt condition of the currently selected device and bit nIEN of the Device Control register.

Note 7: The usage of the DEV bit in the Device/Head register during the access of the task file registers is not defined.

Note 8: Results of performing DMA reads or writes when BSY is set is undefined. The device must not assert DMARQ when BSY is one.

Note 9 Results of performing DMA reads or writes when DRQ is not set is undefined. The device must not assert DMARQ when DRQ is zero.