TO: **John Lohmeyer, Chairman, X3T10 Committee (SCSI)**

From: **Dennis Pak (408)974-4874**
IEEE P1285 Liaison to X3T10/DADI

Date: **September 14, 1994**

Subject: **P1285 Liaison Report for September 1994**

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o Two interface levels: Beta & Gamma
- o Beta Level: One controller, multiple slaves
- o Gamma Level: Multiple masters
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Self-synchronous data transfer
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

* The collaboration with P1596 SCI is progressing well. Another co-located meeting is planned for November.

* A co-located meeting with X3T10 was held in July in New Hampshire. A number of points were brought up including the universality of interfaces, disk array implementations, and the predictability of device latencies.

* The P1285 data structures are being reviewed.

* P1285 is looking into working with the PCI sig on the issue of hot swapping.

Upcoming Events

Future meetings are scheduled as follows:

October 13 Apple Computer, 1 Infinite Loop, Cupertino, CA.
November 3 Quantum Corp, 500 McCarthy Blvd, Milpitas, CA.

Meetings are usually scheduled from 2:00-5:00 PM. Comments and/or questions should be forwarded to Martin Freeman, IEEE P1285 Chair, @(415)354-0329. His e-mail address is martin@savant.PRPA.Philips.COM.