



EXTERNAL MEMO

DATE: August 30, 1994
TO: Membership of X3T10
FROM: Jim McGloth
SUBJ.: WD Command Queuing Proposal

Comments on the WD proposal (ATA/ATAPI Multi Threading, revision 0.1)

I have read the proposal once lightly and have three observations. First, I am withholding comment on the low level signal issues regarding overlapped commands (I have to try out more scenarios first). But on the issue of tagged command queuing I have two comments:

First, tagged command queuing must be offered on ATA as well as ATAPI. Indeed, it is probably more important for disk drives to institute queuing than, say, tape drives. Therefore for the tag value, I propose that it be passed in register 03F3h. This is part of the device control block of registers which is currently decoded by all ATA/ATAPI devices. Most of the registers in this area are used for the floppy disk, with a few for the hard disk. But while 3F2h and 03F4h 8 bit registers are used, 03F3 is not used to my knowledge. 03F3h thus becomes an 8 bit read/write register for the tag value.

Second, I would remove all provisions for tag types in ATA/ATAPI (i.e. head of queue, ordered commands). All queued commands would be treated as simple commands. Based on our SCSI experience, this would greatly simplify the device implementation. And in practice we found little use for head of queue (which really does nothing in the final analysis to insure quick execution of the command) or ordered commands (which are better handled by simply not queuing the command at the drive to begin with). Note that all of this results in a slight shift in complexity from the drive to the driver (i.e. delaying sending down ordered commands), but that is probably the right tradeoff to make.

From "System BIOS for IBM PCs, Compatibles, and EISA Computers" 2nd edition
 1991, Phoenix Technologies

I/O Port List, Continued

I/O Address	Read/Write Status	Description
03D8h*	R/W	CGA mode control register
03D9h*	R/W	CGA palette register
I/O addresses in the 3F2h-3F7h range are primary diskette controller addresses. Bit settings also apply to addresses 0372h-0377h.		
03F2h	W	Diskette controller digital output register, where: Bit 7 = 0 Reserved Bit 6 = 0 Reserved Bit 5 = 1 Drive 1 motor enable Bit 4 = 1 Drive 0 motor enable Bit 3 = 1 Diskette DMA enable Bit 2 = 0 Controller reset Bit 1 = 0 Reserved Bit 0 = 0 Drive 0 select = 1 Drive 1 select
03F4h	R	Diskette controller status register, where: Bit 7 = 1 Data register is ready Bit 6 = 1 Transfer is from controller to system = 0 Transfer is from system to controller Bit 5 = 1 Non-DMA mode Bit 4 = 1 Diskette controller busy Bits 3-2 = Reserved Bit 1 = 1 Drive 1 busy Bit 0 = 0 Drive 0 busy
03F5h	R/W	Diskette controller data register
03F6h	R	Fixed disk control port, where: Bits 7-4 = Reserved Bit 3 = 0 Reduce write current = 1 Head select 3 enable Bit 2 = 1 Disk reset enable = 0 Disk reset disable Bit 1 = 0 Disk initialization enable = 1 Disk initialization disable Bit 0 = Reserved
03F7h	R	Diskette digital input register, where: Bit 7 = 1 Diskette change Bit 6 = 1 Write gate Bit 5 = Head select 3/reduced write current Bit 4 = Head select 2 Bit 3 = Head select 1 Bit 2 = Head select 0 Bit 1 = Drive 1 select Bit 0 = Drive 0 select (Bits 6-0 apply to the currently-selected fixed disk drive)

* For more information on video I/O ports, see the Video I/O Port Lists at the end of this chapter.

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