From: Hale Landis
Subj: ATA rev 2F—section 3.2.5

I recommend that the two identical sentences in this section be changed from "For even values of n from 2 to 512." to "For even values of n starting at 2."

==========

Subj: ATA Rev 2F—sections 4.2 and 4.3

Sorry, I have not been following all the ATA activities as closely as I should the last few months, but...

It seems to me that we had a discussion about sections 4.2 and 4.3 once upon a time and that we were going to move the 2.5" and 1.8" connection info from the annexes into this area of the document. This is a technical thing, but as currently written it would appear that to be "ATA compatible", a device must use the connectors defined in these sections which in the real world are used only by 3.5" and larger drives.

Did I miss something?

==========

Subj: ATA Rev 2f—Section 5.2.4

Again, I may have missed something but I thought that we were going to put in some kind of statement warning host designers against placing improper loading on the DASP- signal because such loading can cause the master/slave handshaking to fail?

==========

Subj: ATA Rev 2f—Section 6.1.1

In the third paragraph, the sentence "When a single device is attached to the interface it shall be set as Device 0." should be deleted.

In the sixth paragraph, last sentence, the word "Typically" is distrubing. It seems to imply that the form of sequential access to sectors on the media is optional. I don't think this form of addressing is optional. I think the word "Typically" should be deleted.

==========

Subj: ATA Rev 2F—Sections 6.2.x

In section 6.2.3, the sentences "*At the end of the command, this register is updated to reflect the current cylinder number.*" and "*At the end of the command, this register is updated to reflect the current LBA bits 16-23.*" should probably be deleted or replaced. A possible replacement could be "*At completion of media access commands, this register may be updated to reflect the high order bits of the last cylinder number accessed.*" and "*At completion of media access commands, this register may be updated to reflect LBA bits 16-23 of the last LBA accessed.*"

In section 6.2.4, the sentences "*At the end of the command, this register is updated to reflect the current cylinder number.*" and "*At the end of the command, this register is updated to reflect the current LBA bits 8-15.*" should probably be deleted or replaced. A possible replacement could be "*At completion of media access commands, this register may be updated to reflect the low order bits of the last cylinder number accessed.*" and "*At completion of media access commands, this register may be updated to reflect LBA bits 8-15 of the last LBA accessed.*"

I recommend that Section 6.2.5 be replaced with the following:

> The data register is either 8-bits or 16-bits depending on the interface width currently selected and/or the type of data being transferred by the current command. This register is used only by PIO data transfer commands.

In section 6.2.6, in the SRST bit description I recommend that the sentence "*Device 1 is not required to execute the DASP- handshake procedure.*"

But what about Device 0? I recommend that this sentence be deleted.

In section 6.2.8, in the L=0 descriptions, the sentence "*At command completion, these bits are updated reflect the currently selected head.*" should probably be deleted or replaced. A possible replacement could be "*At the end of media access commands, these bits may be updated to reflect the last head number accessed.*"

In section 6.2.8, in the L=1 descriptions, the sentence "*At command completion, these bits are updated reflect the current LBA bits 24-27.*" should probably be deleted or replaced. A possible replacement could be "*At the end of media access commands, these bits may be updated to reflect LBA bits 24-27 of the last LBA accessed.*"

In section 6.2.9, I recommend that the descriptions of the MC and MCR bits should be changed to: "*This bit is reserved for use by removable media devices. The use and meaning of this bit is vendor specific.*"

In section 6.2.11, the second paragraph is confusing. It implies that a host need only check this register to determine if a command was successful which is not true—the Status register should be used to make this determination. I recommend this paragraph be replaced with: "*For media access commands, this register shall be zero at the completion of a command if there is no error indication in the Status register. For media access commands that complete with an error indication in the Status register, this register contains the number of sectors which need to be transferred in order to complete the request.*"

Section 6.2.12, is confusing with respect to the contents of the register at command completion. I recommend that this section be replaced with: "For media access commands in CHS mode, this register contains the starting sector number. For media access commands in LBA mode, this register contains bits 0-7 of the starting LBA."

This register is used by some non-media access commands to pass command specific information to the device. At the completion of media access commands in CHS mode, this register may be updated to reflect the last sector number accessed. At the completion of media access commands in LBA mode, this register may be updated to reflect bits 0-7 of the last LBA accessed. This register is used by some non-media access commands to pass command specific to the host.

==========

Subj: ATA Rev 2F—Section 6.2.13, etc

Oh boy, its Status register time and of all the 6.2.x sections this one is the biggest problem. It is much less work if I just propose a complete rewrite of this section and also propose a new section, so here goes...

First, please note that I have deleted some of the references to the old status being valid within 400ns of BSY=0 -- this *MUST* go away—an ATA device *MUST* make its status valid *BEFORE* BSY=0 if host software people are going to be able to program this interface on faster systems!

Here is my proposed rewrite of section 6.2.13. Please read this carefully—thanks!

6.2.13. Status register

This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device. When BSY=0, the other bits in this register are valid and the other Command Block register may contain meaningful information. When BSY=1, no other bits in this register are valid and no other Command Block registers contain any meaningful information. For devices that implement the Power Management features, the contents of the Status register, and all other Command Block registers, is unpredictable while a device is in the Sleep power saving mode.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge and the interrupt is cleared.

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

BSY (Busy) is set whenever the device has control of the Command Block Registers. When BSY=1, a read of any Command Block Register shall return the contents of the Status register.

The device shall not change the state of the DRQ, CORR or ERR bits unless BSY=1, except when the last sector of a PIO data in command has been transferred by the host the DRQ bit is cleared without the BSY bit being set.

The BSY bit is set by the device under the following circumstances:

a) within 400 nsec after the negation of RESET- or after SRST has been set in the Device Control register.
b) within 400 nsec after a write of the Command register.
c) during data transfer phase of PIO data in commands if there is another sector or block to transfer.
d) during data transfer phase of PIO data out commands following the transfer of a sector or block.
e) during the data transfer phase of DMA commands.

The BSY bit remains set until the reset activity is completed.

For commands, either the BSY bit must be set, or if the BSY bit is cleared, the DRQ bit must be set, until command completion.

DRDY (Device Ready) is set to indicate that the device is capable of responding to and attempting to execute all possible commands codes. Devices that implement the power management features maintain DRDY=1 when they are in the Idle and Standby power saving modes. When the state of the DRDY bit changes, it shall not change again until after the host reads the Status register.

During any time when DRDY=0 a device must respond as follows to commands:

a) the device shall accept and attempt to execute the EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS commands.
b) the device should reject all other commands codes by setting the ABRT bit in the Error register and setting the ERR bit in the

Status register before clearing the BSY bit to signal command completion. If a device accepts commands other than EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS during the time DRDY=0, the results are vendor specific.

DWF (Device Write Fault) indicates a write fault error has been detected. The internal status or internal conditions that causes this error to be indicated is vendor specific. When the state of the DWF bit changes, it shall not change again until after the host reads the Status register.

DSC (Device Seek Complete) is set to indicate that the device has completed all activities associated with a seek operation. A device may clear this bit at the start of a seek operation and set this bit at the completion of a seek operation. The SEEK command normally consists of only a seek operation, but seek operations may be part of the functions performed by other commands. If a device does not implement a seek operation or does not indicate the status of seek operations, this bit shall have the same value as the DRDY bit. When the state of the DSC bit changes, it shall not change again until after the host reads the Status register.

DRQ (Data Request) indicates that the device is ready to transfer data between the host and the device. The DRQ bit is not used and remains cleared during the execution of non-data transfer commands. During execution of PIO data transfer commands and DMA commands, either the BSY bit must be set, or if the BSY bit is cleared, the DRQ bit must be set, until command completion.

The state of the DRQ bit shall not change during PIO commands except as follows:

a) During PIO data transfer commands when the device is prepared to transfer data the DRQ bit shall be set before the BSY bit is cleared.
b) During PIO data transfer commands when the host has transferred the current sector or block and there is another sector or block to transfer the BSY bit shall be set before the DRQ bit is cleared.
c) Following the transfer of the last sector or block of a PIO data in command, the DRQ bit shall be cleared while the BSY bit also remains cleared. The DRQ bit is cleared by a reset and by a host write to the Command register.

CORR (Corrected Data) indicates that a correctable data error was encountered and that the data has been corrected by the device. This condition does not terminate the current command. The conditions that cause the CORR bit to be set are vendor specific. The CORR may be set and cleared at any time during the execution of a data transfer command, but if it is set one or more times during the execution of a data transfer command, it shall be set prior to the last time the BSY bit is cleared for the command. The CORR bit is cleared by a reset and by a host write to the Command register. It is recommended that host software ignore this bit.

IDX (Index) is vendor specific.

ERR (Error) indicates that an error occurred during the execution of a command and that the contents of the Error register are valid. The ERR bit shall remain set and the Error register contents shall remain valid until cleared by a reset or by a host write to the Command register.

I propose that the following new section be added. I'm not sure 6.2.14 is the "correct" section number. And I know many of you are going to ask why this such a mess—why are there two methods? Please refer to the strange little note near the beginning of the existing section 6.2.13...

Note: If Device 1 is not detected as being present, Device 0 clears the Device 1 Status register to 00H (indicating that the device is Not Ready).

This strange little note is the *ONLY* comment in the document that describes this condition. This note has resulted in implementations that worked as described by the second method.

6.2.14 Single device configurations

In a single device configuration where device 0 is the only device and the host selects device 1, device 0 may respond to accesses of the Command Block and Control Block registers in one of two methods. These two methods exist because previous versions of the ATA standard did not specify the required behaviour for this configuration.

The first method requires that device 0 implement an Error, Status and Alternate Status register that is used whenever device 1 is selected. The first method is the recommended implementation. The first method is:

1) The device 1 Error, Status and Alternate status registers are set to 00H by a reset.
2) A write to the Device Control register shall complete as if device 0 was the selected device.
3) A write to the Command Block register, other than the Command register, shall complete as if device 0 was selected.
4) A write to the Command command register with a command code other than the INITIALIZE DEVICE PARAMETERS or EXECUTE DEVICE DIAGNOSTICS command causes the device 1 Error, Status and Alternative status registers to be used as follows:
   a) the BSY bit is set in the device 1 status registers.
   b) the ABRT bit is set in the device 1 Error register.
   c) the ERR bit is set in the device 1 status registers.
   d) the BSY bit is cleared in the device 1 status registers.
   e) if the nIEN bit in the Device Control Register is cleared, the INTRQ signal is asserted.
5) An EXECUTE DEVICE DIAGNOSTIC command is executed as if it addressed to device 0.
6) An INITIALIZE DEVICE PARAMETERS command is executed as if device 1 is present and is actually executing the command. The command shall have no effect of the device parameters of device 0.

[Editors note: Why is this you ask? Because this command is *NOT* allowed to set the ERR bit in the Status register at any time or for any reason!]

7) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if device 0 was selected.
8) A read of the Error, Status or Alternate status register returns the value in the device 1 copy of these registers. The device 1 status registers will contain 00H following a reset and the value 01H following an attempt to execute a command, other than EXECUTE DEVICE DIAGNOSTICS or INITIALIZE DEVICE PARAMETERS, on device 1.

The second method is:

1) A write to the Device Control register shall complete as if device 0 was the selected device.
2) A write to the Command Block register, other than the Command register, shall complete as if device 0 was selected.
3) A write to the Command command register is ignored.
5) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if device 0 was selected.
6) A read of the Status or Alternate status register returns the value 00H.

In a single device configuration where device 1 is the only device and the host selects device 0, device 1 shall respond to accesses of the Command Block and Control Block registers in the same way it would if device 0 was present. This is because device 1 can not determine if device 0 is, or is not, present.

==========

Subj: ATA Rev 2F—Section 7.1

Ahhh... Here it is again... That strange statement about what Device 0 does when there is no Device 1...

I recommend that the sentence "*If Device 0 does not detect DASP- during the reset sequence above, then Device 0 shall respond to a PIO read of the status Register of Device 1 with a value of 00h.*" be replace by "*If Device 0 does not detect DASP- during the reset sequence above, then Device 0 shall respond to a write and read operations of the Device 1 Command Block and Control Block registers as described in section 6.2.14.*"

Note that section 6.2.14 is my proposed new section—the section number is subject to change.

==========

Subj: ATA Rev 2F—Section 7.2

Section 7.2, all two sentences of it, are the entire discussion of translation modes in the ATA-2 document. I think this topic needs much more definition than these two sentences. Therefore, I propose the following changes/additions to this section. First I recommend that the 5th, 6th, 7th and 8th paragraphs in section 6.1.1 be deleted. Currently section 6.1.1 starts out talking about "addressing modes" with respect to the Command Block and Control Block registers and then in the 5th paragraph is switches to talking about sector addressing—very confusing. So here is my recommended rewrite of section 7.2.

7.2 Sector addressing modes

All addressing of data sectors recorded on the device's media is by a logical sector address. The mapping of logical sector addresses to the actual physical location of the data sector on the media is vendor specific.

An ATA device shall support at least one logical CHS translation mode known as the default translation mode. The device shall enter this translation mode following a reset. A device may support other logical translation modes and the host may use the INITIALIZE DEVICE PARAMETERS command to select the default CHS mode or any of the other supported CHS modes. The default translation mode is described in the Identify Device information.

The current translation mode may also be described in the Identify Device information.

A CHS address is made up of three fields: the sector address, the head number and the cylinder number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255. Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but can not exceed 15. Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65,535.

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

Sequential access to logical sectors shall be accomplished by treating the sector number as the least significant portion of the address, the head number as the middle portion of the address and the cylinder number as the most sigificant portion of the address.

A device may also support the optional LBA mode of addressing. A device that supports LBA mode indicates this in the Identify Device information. A host shall not attempt to use LBA mode unless the device indicates the mode is supported.

If a device supports LBA addressing mode, then the following shall be supported by the device:

1) The host may select either CHS addressing in the current translation mode or LBA addressing on a command-by-command basis by using the LBA bit in the Device/Head register.
2) A command must complete in the same addressing mode as selected by the host at command initiation.
3) When LBA mode is selected by the host, the Sector Number register, Cylinder Low register, Cylinder High register and bits HS3-HS0 of the Device/Head register contain an LBA mode address.
4) LBA mode must be supported for all media access commands, except for the FORMAT TRACK command. The LBA bit of the Device/Head register shall be ignored for commands that do not access the media.
5) Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true (heads_per_cylinder and sectors_per_track are the current translation mode values):
   LBA = ((cylinder * heads_per_cylinder + heads) sectors_per_track) + sector - 1

==========

Subj: ATA Rev 2F—Section 8 -- general comments

Many months ago I said I would rewrite what is now section 8, the command descriptions. I said I would do this in the style I used for the rewrite of the power management commands.

OK... I'm doing it now. Expect to see several messages, each containing a part of section 8, probably 5-10 commands per message.

And, my recent complaint that while my new power management introduction stuff got into ATA-2, my new power management command descriptions did not get into ATA-2, is true. Well.I'm going to fix that in my rewrite. Are you ready? (I'm not sure I am, but here goes...)

8. Command Descriptions

Commands are issued to the device by loading the pertinent

registers in the command block with the needed parameters, and then writing the command code to the Command register.

The manner in which a command is accepted varies. There are three classes (see table 10) of command acceptance, all predicated on the fact that to receive a command, BSY=0:

```
################################################################
#
#Hale's note:  I think all this command class stuff is a bunch
#of junk, especially Classes 2 and 3. I think these should be
#removed and all replaced by a statement like:
#
#Upon receipt of a command, the device sets BSY within 400
#nsec.  Following BSY=1, the status presented by the device
#depends on the type of command:  PIO data in, PIO data out,
#non-data transfer or DMA.  See the individual command
#descriptions and Section 9 for the protocol followed by each
#command and command type.
#
#Next I would replace the class column in table 10 with a
#type column (PIO, DMA, non-data)
#
################################################################
```

- Upon receipt of a Class 1 command, the device sets BSY within 400 nsec.
- Upon receipt of a Class 2 command, the device sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 usec, and clears BSY within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the device sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec, and clears BSY within 400 nsec of setting DRQ.

NOTE: DRQ may be set so quickly on Class 2 and Class 3 that the BSY transition is too short for BSY=1 to be recognized.

```
################################################################
#
#Hale's note:  I have replaced the "class" column with the
#"protocol" column and labeled the "type" column so you can see #what I mean.
#
################################################################
```

The proto column codes represent the command protocol used:

DM - A DMA command.
ND - A non data command.
PI - A PIO data in command.
PO - A PIO data out command.

VS - A Vendor specific command.

The typ column codes represent the command type:

O - Optional—the implementation of this command is optional.
M - Manadatory—all ATA devices must implement this command.
R - Reserved for use in future ATA standards.
V - Reserved for vendor specific use.

proto		typ	Command code	FR	SC	SN	CY	DH
VS	ACKNOWLEDGE MEDIA CHANGE	O	DBh					D
VS	BOOT - POST-BOOT	O	DCh					D
VS	BOOT - PRE-BOOT	O	DDh					D
ND	CHECK POWER MODE	O	98h E5h		y			D
VS	DOOR LOCK	O	DEh					D
VS	DOOR UNLOCK	O	DFh					D
PO	DOWNLOAD MICROCODE	O	92h	y	y	y	y	D
ND	EXECUTE DEVICE DIAGNOSTIC	M	90h					D*
PO	FORMAT TRACK	M	50h	*	y		y	y
PI	IDENTIFY DEVICE	M	ECh					D
ND	IDLE	O	97h E3h		y			D
ND	IDLE IMMEDIATE	O	95h E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	91h		y			y
ND	NOP	O	00h					y
PI	READ BUFFER	O	E4h					D
DM	READ DMA (w/retry)	O	C8h		y	y	y	y
DM	READ DMA (w/o retry)	O	C9h		y	y	y	y
PI	READ LONG (w/retry)	M	22		y	y	y	y
PI	READ LONG (w/o retry)	M	23		y	y	y	y
PI	READ MULTIPLE	O	C4h		y	y	y	y
PI	READ SECTOR(S) (w/retry)	M	20		y	y	y	y
PI	READ SECTOR(S) (w/o retry)	M	21		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/retry)	M	40		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/o retry)	M	41		y	y	y	y
ND	RECALIBRATE	M	1xh					D
ND	SEEK	M	7xh				y	y
ND	SET FEATURES	O	EFh	y				D
ND	SET MULTIPLE MODE	O	C6h		y			D
ND	SLEEP	O	99h E6h					D
ND	STANDBY	O	96h E2h		y			D
ND	STANDBY IMMEDIATE	O	94h E0h					D
PO	WRITE BUFFER	O	E8h					D
DM	WRITE DMA (w/retry)	O	CAh		y	y	y	y
DM	WRITE DMA (w/o retry)	O	CBh		y	y	y	y
PO	WRITE LONG (w/retry)	M	32	*	y	y	y	y
PO	WRITE LONG (w/o retry)	M	33	*	y	y	y	y
PO	WRITE MULTIPLE	O	C5h	*	y	y	y	y
PO	WRITE SAME	O	E9h	y	y	y	y	y
PO	WRITE SECTOR(S) (w/retry)	M	30	*	y	y	y	y
PO	WRITE SECTOR(S) (w/o retry)	M	31	*	y	y	y	y
PO	WRITE VERIFY	O	3Ch	*	y	y	y	y
VS	Vendor specific	V	9Ah					
VS	Vendor specific	V	C0-C3h					
VS	Vendor specific	V	8xh					
VS	Vendor specific	V	F0h-FFh					
--	Reserved: all remaining codes	R						

CY = Cylinder registers SC = Sector Count register
DH = Device/Head register SN = Sector Number register
FR = Features register (see command descriptions for use)
y - the register contains a valid parameter for this command.
For the Device/Head register, y means both the device and head parameters are used.
D - only the device parameter is valid and not the head parameter.
D* - Addressed to device 0 but both devices execute it.
* - Maintained for compatibility (see 6.2.10)

1.1.1.1.1.1.1.1.1 Table 10 - Command Codes and Parameters (Part 2 of 2)

Each command description in the following sections contain the following subsections:

TYPE - Indicates if the command is manadatory or optional.

PROTOCOL - Indicates which protocol is used by the command. INPUTS - Describes the Command Block register data that the host must supply.

OUTPUTS - Describes the Command Block register data that is returned by the device at the end of a command.

PREREQUISITES - Any prerequisite commands or conditions that must be meet before the command can be issued.

DESCRIPTION - The description of the commands function(s). ERRORS - Describes the error conditions that may cause the command to fail.

```
#########################################################################
#
#Hale's note: At one of the meeting I suggested that the "removable
#media" commands be made Vendor Specific.  I have done that here.
#
#These commands were never properly described and there are few but
#very different implementations of these commands.  So why not make
#them VS?
#
#########################################################################
```

8.1. ACKNOWLEDGE MEDIA CHANGE (removable)

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

ERRORS - If the device does not support this command, the device returns a Command Abort error. All other error conditions are vendor specific.

8.2. BOOT - POST-BOOT (removable)

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

ERRORS - If the device does not support this command, the device returns a Command Abort error. All other error conditions are vendor specific.

8.3. BOOT - PRE-BOOT (removable)

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

ERRORS - If the device does not support this command, the device returns a Command Abort error. All other error conditions are vendor specific.

8.4. CHECK POWER MODE

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

OUTPUTS - The Sector Count register is set to 0 (00h) if the device is going to, in or leaving Standby mode. The Sector Count register is set to 255 (FFh) if the device is in Active or Idle mode.

PREREQUISITES - None.

DESCRIPTION - If the device is in, going to, or recovering from the Standby Mode the device shall set BSY, set the Sector Count register to 0 (00h), clear BSY, and assert INTRQ.

If the device is in Active or Idle Mode, the device shall set BSY, set the Sector Count register to 255 (FFh), clear BSY, and assert INTRQ.

ERRORS - Command abort if the device does not support the Power Management command set.

8.5. DOOR LOCK (removable)

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

ERRORS - If the device does not support this command, the device returns a Command Abort error. All other error conditions are vendor specific.

8.6. DOOR UNLOCK (removable)

TYPE - Optional.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

ERRORS - If the device does not support this command, the device returns a Command Abort error. All other error conditions are vendor specific.

8.7. DOWNLOAD MICROCODE

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The head bits of the Device/Head register shall always be set to zero. The Cylinder High and Low registers shall be set to zero. The Sector Number and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number Register and the Sector Count register. The Sector Number Register shall be used to extend the Sector Count register, to create a sixteen bit sector count value. The Sector Number Register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number Register and the Sector Count register shall indicate no data is to be transferred. This allows transfer sizes from 0 bytes to 33 553 920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Feature Register are:

01H - download is for immediate, temporary use
07H - save downloaded code for immediate and future use
All other values are reserved.

ERRORS - Command Abort if the device does not support this command. All other error conditions are vendor specific.

8.8. EXECUTE DEVICE DIAGNOSTIC

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - None, except that the device selection bit in the Device/Head register is ignored.

OUTPUTS -The diagnostic code written to the Error register is a unique 8-bit code as shown in table 11, and not as the single bit flags defined in 7.2.9. If Device 1 fails diagnostics, Device 0 "OR's" 80h with its own status and loads that code into the Error register. If Device 1 passes diagnostics or there is no Device 1 connected, Device 0 "OR's" 00h with its own status and loads that code into the Error register.

Code	
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controlling microprocessor error
8xh	Device 1 failed

1.1.1.1.1.1.1.1.2 Table 11 - Diagnostic Codes

PREREQUISITES - None.

```
############################################################
#
#Hale's note:  The description of this command has never been
#correct (or even made any sense!).  I think I've fixed that #here.
#
############################################################
```

DESCRIPTION - This command shall perform the internal diagnostic tests implemented by the device. See also clauses 6.2.4 and 6.2.13. The DEV bit is ignored. Both devices, if present, shall execute this command.

If Device 1 is present, it performs the following functions:

a) Drive 1 sets BSY within 400 nsec after the EXECUTE DEVICE DIAGNOSTIC command was received.
b) Drive 1 negates PDIAG- within 1 msec after command received.
c) Drive 1 performs internal diagnostics.

d) Drive 1 posts diagnostic results to the Error Register
e) Drive 1 clears BSY when ready to accept commands that do not require DRDY=1.
f) Drive 1 asserts PDIAG- to indicate that it is ready to accept commands.
NOTE: Drive 1 must clear BSY and assert PDIAG- within 5 seconds from the time that the EXECUTE DEVICE DIAGNOSTIC command was received.

g) Drive 1 sets DRDY when ready to accept any command.
NOTE: Steps e), f) and g) may occur at the same time.

If Device 0 is present, it performs the following functions:

a) Drive 0 sets BSY within 400 nsec after the EXECUTE DEVICE DIAGNOSTIC command was received.
b) Drive 0 performs internal diagnostics.
c) Drive 0 waits up to 6 seconds for Drive 1 to assert PDIAG-.
d) Drive 0 posts diagnostic results to the Error Register
e) Drive 0 clears BSY when ready to accept commands that do not require DRDY=1.
NOTE: Drive 0 must clear BSY within 6 seconds from the time that the EXECUTE DEVICE DIAGNOSTIC command was received.

f) Drive 0 sets DRDY when ready to accept any command.
NOTE: Steps e) and f) may occur at the same time.

ERRORS - None. All error information is returned as a diagnostic code in the Error register.

8.9. FORMAT TRACK

TYPE - Manadatory.

PROTOCOL - PIO data out.

INPUTS - Vendor specific.

OUTPUTS - Vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - The implementation of the FORMAT TRACK command is vendor specific. It is recommend that system implementations not utilize this command.

ERRORS - Vendor specific.

8.10. IDENTIFY DEVICE

TYPE - Manadatory

PROTOCOL - PIO data in.

INPUTS - None.

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

When the command is issued, the device sets BSY, prepares to transfer the 256 words or device identification data to the host, sets DRQ, clears BSY, and generates an interrupt. The host can then transfer the data by reading the Data register. The parameter words in the buffer have the arrangement and meanings defined in Table 12. All reserved bits or words shall be zero. The F/V column indicates if the word or part of a word has fixed (F) contents that do not change, variable (V) contents that may change depending on the device state or the commands executed by the device, X for words with vendor specific data which may be fixed or variable, and R for reserved words which shall be zero.

ERRORS - None.

Word		F/V
0	General configuration bit-significant information:	
	15 0 reserved for non-magnetic devices	F
	14 Vendor specific (obsolete)	F
	13 Vendor specific (obsolete)	F
	12 Vendor specific (obsolete)	F
	11 Vendor specific (obsolete)	F
	10 Vendor specific (obsolete)	F
	9 Vendor specific (obsolete)	F
	8 Vendor specific (obsolete)	F
	7 1=removable cartridge device	F
	6 1=fixed device	F
	5 1=spindle motor control option implemented	F
	4 Vendor specific (obsolete)	F
	3 Vendor specific (obsolete)	F
	2 Vendor specific (obsolete)	F
	1 Vendor specific (obsolete)	F
	0 0=reserved	F
1	Number of cylinders	F
2	Reserved	R
3	Number of heads	F
4	Vendor specific (obsolete)	X
5	Vendor specific (obsolete)	X
6	Number of sectors per track	F
7-9	Vendor specific	X
10-19	Serial number (20 ASCII characters, 0000h=not specified)	F
20	Vendor specific (obsolete)	X
21	Buffer size in 512 byte increments (0000h=not specified)	F
22	# of vendor specific bytes avail on READ/WRITE LONG cmds	F
	(0000h=not spec'd)	
23-26	Firmware revision (8 ASCII characters, 0000h=not specified)	F
27-46	Model number (40 ASCII characters, 0000h=not specified)	F
47	15-8 Vendor specific	X
	7-0 00h = READ/WRITE MULTIPLE commands not implemented	F
	xxh = Maximum number of sectors that can be transferred	F
	per interrupt on READ AND WRITE MULTIPLE commands	
48	0000h = cannot perform doubleword I/O	F
	0001h = can perform doubleword I/O	F
49	Capabilities	
	15-13 0=reserved	R
	12 1=Reserved (for advanced PIO mode support)	R
	11 1=IORDY supported	F
	0=IORDY may be supported	F
	10 1=IORDY can be disabled	F
	9 1=LBA supported	F
	8 1=DMA supported	F
	7- 0 Vendor specific	X
50	Reserved	R
51	15-8 PIO data transfer cycle timing mode	F
	7-0 Vendor specific	X
52	15-8 DMA data transfer cycle timing mode	F
	7-0 Vendor specific	X
53	15-2 Reserved	R
	1 1=the fields reported in words 64-70 are valid	F
	0=the fields reported in words 64-70 are not valid	F
	0 1=the fields reported in words 54-58 are valid	F
	0=the fields reported in words 54-58 may be valid	F
54	Number of current cylinders	V
55	Number of current heads	V

56	Number of current sectors per track	V
57-58	Current capacity in sectors	V
59	15-9 Reserved	R
	8 1 = Multiple sector setting is valid	V
	7-0 xxh = Current setting for number of sectors that can be transferred per interrupt on R/W multiple command	V
60-61	Total number of user addressable sectors (LBA mode only)	F
62	15-8 Single word DMA transfer mode active	V
	7-0 Single word DMA transfer modes supported	F
63	15-8 Multiword DMA transfer mode active	V
	7-0 Multiword DMA transfer modes supported	F
64	15-8 Reserved	R
	7-0 Advanced PIO Transfer Modes Supported	F
65	Minimum Multiword DMA Transfer Cycle Time Per Word	
	15-0 Cycle time in nanoseconds	F
66	Manufacturer's Recommended Multiword DMA Transfer Cycle Time	
	15-0 Cycle time in nanoseconds	F
67	Minimum PIO Transfer Cycle Time Without Flow Control	
	15-0 Cycle Time in nanoseconds	F
68	Minimum PIO Transfer Cycle Time With IORDY Flow Control	
	15-0 Cycle Time in nanoseconds	F
69-70	Reserved (for advanced PIO mode support)	R
71-127	Reserved	R
128-159	Vendor specific	X
160-255	Reserved	R

1.1.1.1.1.1.1.1.3 Table 12 - Identify Device Information (Part 2 of 2)

[Editor's Note: There are currently restrictions by some operating systems and BIOSs that make it desireable to set limits or impose restrictions on some of the parameters returned by the Identify Device command. These restrictions are not currently included in this proposal and must be addressed before this document is complete.]

```
############################################################
#
#Hale's note:  As you may recall I asked that each word be
#described in sections 8.10.x—I have done this here.
#
############################################################
```

8.10.1. Word 1: Number of cylinders

The number of user-addressable cylinders in the default translation mode.

8.10.2. Word 2: Reserved.

8.10.3. Word 3: Number of heads

The number of user-addressable heads in the default translation mode.

8.10.4. Word 4: Vendor specific data.

8.10.5. Word 5: Vendor specific data.

8.10.6. Word 6: Number of sectors per track

The number of user-addressable sectors per track in the default translation mode.

8.10.7. Words 7-9: Vendor specific data.

8.10.8. Words 10-19: Serial Number

The contents of this field are right justified and padded with spaces (20h).

8.10.9. Word 20: Vendor specific data.

8.10.10. Word 21: Buffer size.

The size of the device buffer in 512-byte increments:

0000H = not specified
0001H = 512 bytes
0002H = 1024 bytes

8.10.11. Word 22: Vendor specific bytes on READ/WRITE LONG commands

If the contents of this field are set to a value other than 4, the only way to use this information is via the SET FEATURES subcommand that enables more than 4 bytes to be transferred.

8.10.12. Word 23-26: Firmware revision

The contents of this field are left justified an padded with spaces (20h).

8.10.13. Words 27-46: Model number

The contents of this field are left justified and padded with spaces (20h).

8.10.14. Word 47: READ/WRITE MULTIPLE support.

Bits 7-0 of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands. If a device supports the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits contain a non-zero value. If the device does not support the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits shall be zero.

8.10.15. Word 48: Double Word I/O support.

This word is not used by ATA-2 devices and shall be set to zero.

8.10.16. Word 49: Capabilities

8.10.16.1. IORDY Support

Bit 11 of word 49 is used to help determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This insures backward compatibility.

If a device supports PIO Mode 3, then this bit must be set.

8.10.16.2. IORDY Can Be Disabled

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY.

8.10.16.3. LBA supported

Bit 9 of word 49 is used to indicate if the device supports LBA mode addressing. If this bit is set, words 60-61 must be valid.

8.10.16.4. DMA supported

Bit 9 of word 49 is used to indicate if the device supports the READ/WRITE DMA commands.

8.10.17. Word 50: Reserved.

8.10.18. Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 5 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 2 categories specified in figure 5, and if it does not, then Mode 0 shall be used to serve as the default timing. Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

8.10.19. Word 52: Single Word DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 6 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 6 (i.e. 0, 1, or 2), and if it does not, then Mode 0 shall be used to serve as the default timing.

The contents of this word shall be ignored if Words 62 or 63 are supported.

8.10.20. Word 53: Field Validity

Word 53, bit 0 defines whether the fields contained in words 54 through 58 are guaranteed to be valid. If this bit is not set, the fields contained in words 54 through 58 may be valid. Word 53, bit 1 will be set if any of the fields reported in words 64 through 70 are valid. This bit will be reset if the fields reported in words 64-70 are not valid. Any device which supports PIO Mode 3 or above, or supports Multiword DMA Mode 1 or above, must set bit 1 of word 53 and support the fields contained in words 64 through 70.

8.10.21. Word 54: Number of current cylinders

The number of user-addressable cylinders in the current translation mode.

8.10.22. Word 55: Number of current heads

The number of user-addressable heads in the current translation mode.

8.10.23. Word 56: Number of current sectors per track

The number of user-addressable sectors per track in the current translation mode.

8.10.24. Word 57-58: Current capacity in sectors

The current capacity in sectors excludes all sectors used for device-specific purposes. The number of sectors of available capacity shall be calculated as:

(Number of current cylinders) * (Number of current heads) * (Number of current sectors per track)

8.10.25. Word 59: Multiple sector setting

If bit 8 is set, then bits 7-0 reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. If word 47 bits 7-0 are zero then word 59 bits 8-0 shall also be zero.

8.10.26. Word 60-61: Total number of user addressable sectors

If the device supports LBA Mode, these words reflect the total number of user addressable sectors. This value does not depend on the current device geometry. If the device does not support LBA mode, these words shall be set to 0.

8.10.27. Word 62: Single word DMA transfer

The low order byte identifies by bit all of the Modes which are supported e.g. if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

8.10.28. Word 63: Multiword DMA transfer

The low order byte identifies by bit all of the Modes which are supported e.g. if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

8.10.29. Word 64: Flow Control PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes that it is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3. Bit 1, if set, indicates that the device supports PIO Mode 4.

> Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

8.10.30. Word 65: Minimum Multiword DMA Transfer Cycle Time Per Word

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 must be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time reported by the fastest DMA mode supported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.31. Word 66: Manufacturer's Recommended Multiword DMA Cycle Time

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the Manufacturer's Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance MAY result.

If this field is supported, bit 1 of word 53 must be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.32. Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

Word 67 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer Without Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above must support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.33. Word 68: Minimum PIO Transfer Cycle Time With IORDY

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer With IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 must be set.

Any device which supports PIO Mode 3 or above must support this field, and the value in word 68 shall not be less than the fastest PIO mode reported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.34. Words 69-70: Reserved for future PIO modes.

Words 69 and 70 are reserved for future advanced PIO modes. (Editor's note: It is intended that this field be used for future specification of an alternative flow control mechanism, currently being referred to as advanced PIO flow control.)

8.10.35. Words 71-127: Reserved.

Words 69 and 70 are reserved for future advanced PIO modes.

8.10.36. Words 128-159: Reserved.

8.10.37. Words 160-255: Vendor specific.

8.11. IDLE

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby Timer. See Table 13.

+----------+----------+

Sector Count Register contents	Corresponding Timeout Period
0 (00h)	Timeout Disabled
1 - 240 (01h-F0h)	(value * 5) seconds
241 - 251 (F1h-FBh)	((value - 240) * 30) minutes
252 (FCh)	21 minutes
253 (FDh)	Vendor unique period between 8 and 12 hours
254 (FEh)	Reserved
255 (FFh)	21 minutes 15 seconds

1.1.1.1.1.1.1.1.4 Table 13 - Automatic Standby Timer Periods

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set BSY, enter the Idle Mode, clear BSY, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

ERRORS - Command Abort - The device does not support the Power Management command set.

8.12. IDLE IMMEDIATE

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set BSY, enter the Idle Mode, clear BSY, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

ERRORS - Command Abort - The device does not support the Power Management command set.

8.13. INITIALIZE DEVICE PARAMETERS

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Sector Count register specifies the number of sectors per track, and the Device/Head register which specifies the number of heads minus 1.

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder for the current CHS translation mode.

Upon receipt of the command, the device sets BSY, saves the parameters, clears BSY, and generates an interrupt.

The sector and head values are not checked for validity by this command. If they are invalid, no error will be posted until an attempt is made to execute a media access command which shall be failed with an ID Not Found error.

ERRORS - None. This command is not allow to fail or set any errors conditions for any reason.

8.14. NOP

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - None.

OUTPUTS - The Command Block registers, other than the Error and Status registers, are not changed by this command. PREREQUISITES - None.

DESCRIPTION - This command enables a host which can only perform 16-bit register accesses to check device status. The device shall respond as it does to an unrecognized command by setting Abort in the Error register, Error in the Status register, clearing Busy in the Status register, and asserting INTRQ. NOTE: When a 16-bit host writes to the Device/Head Register, one byte contains the Command register, so the device sees a new command when the intended purpose is only to select a device. Both devices may be Busy but not necessarily Ready, e.g. Device 0 may be ready, but not device 1. To check this possibility a typical sequence for an 8-bit host would be:

a) Read the Status register (wait until Busy False)
b) Select the device (write to the Device/Head Register)
c) Read the Status register (wait until Busy False and Ready True)
d) Send the command (write to the Command register).

As a 16-bit host executes b and d simultaneously, a problem occurs if the device being selected is Not Ready at the time the command is issued.

ERRORS - This command always fails with a Command Abort error.

8.15. READ BUFFER

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - None.

OUTPUTS - None.

PREREQUISITES - A WRITE BUFFER command should immediately preceed a READ BUFFER command.

DESCRIPTION - The READ BUFFER command enables the host to read the current contents of the device's sector buffer. When this command is issued, the device sets BSY, sets up the sector buffer for a read operation, sets DRQ, clears BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

ERRORS - Command Abort if the command is not supported.

8.16. READ DMA

TYPE - Optional.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred or the address of the sector where the first error was detected.

PREREQUISITES - The host must initialize a slave-DMA channel.

DESCRIPTION - This command executes in a similar manner to the

READ SECTOR(S) command except for the following:

- the host initializes a slave-DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a Read DMA command, the device shall provide status of BSY or DRQ until the command is completed.

At command completion, the Command Block Registers contain the sector address of the last sector transferred.

An unrecoverable error encountered during execution of a READ DMA command results in the termination of the command. At command completion, the Command Block Registers contain the sector address of the sector where the first error occurred. ERRORS - Command Abort if the command is not supported. Other errors possible are Bad Block, Uncorrectable data error, ID Not Found and Address Mark Not Found.

8.17. READ LONG

TYPE - Manadatory.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be read. The Sector Count register shall not specify a value other than 1.

OUTPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred or the address of the sector where the first error was detected.

PREREQUISITES - The SET FEATURES subcommand to enable more than 4 vendor specific bytes must be executed prior to the READ LONG command if more than 4 vendor specific bytes are to be transferred. DESCRIPTION - The READ LONG command performs similarly to the READ SECTOR(S) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector. During a READ LONG command, the device does not check to determine if there has been a data error. Only single sector read long operations are supported.

The transfer of the vendor specific bytes shall be one byte at a time over bits DD0-7 only (8-bits wide).

ERRORS - Bad Block, ID Not Found Command Abort and Address Mark Not Found.

8.18. READ MULTIPLE command

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - If not error, the Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred. These registers are undefined if an error condition is indicated at command completion. PREREQUISITES - A successful SET MULTIPLE MODE command must preceed a READ MULTIPLE command.

DESCRIPTION - The READ MULTIPLE command performs similarly to the READ SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command. Command execution is identical to the READ SECTOR(S) operation except that the number of sectors defined by a SET MULTIPLE MODE command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the READ MULTIPLE command. When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where n = Remainder (SECTOR COUNT / block count)

If the READ MULTIPLE command is attempted before the SET MULTIPLE MODE command has been executed or when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with an Aborted Command error.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

ERRORS - Bad Block, Uncorrectable Data Error, ID Not Found Command Abort and Address Mark Not Found.

8.19. READ SECTOR(S)

TYPE - Manadatory.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - If no error, the Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred. If the comamnd ends with an error, these registers contain the address of the sector where the first error was detected and the Sector Count register contains the number of sectors remaining to be transferred in order to complete the original request.

PREREQUISITES - None.

DESCRIPTION - This command reads from 1 to 256 sectors as specified in the Sector Count register. A SECTOR COUNT of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

If the device is not already on the desired track, an implied seek is performed.

DRQ is always set prior to data transfer regardless of the presence or absence of an error condition.

The types of errors that are not retried when no retries is requested by the host is vendor specific.

ERRORS - Bad Block, Uncorrectable Data Error, ID Not Found Command Abort and Address Mark Not Found.

8.20. READ VERIFY SECTOR(S)

TYPE - Manadatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be verified. The Sector Count register specifies the number of sectors to be verified.

OUTPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector verified or the address of the sector where the first error was detected. PREREQUISITES - None.

DESCRIPTION - This command is identical to the READ SECTOR(S) command, except that DRQ is never set, and no data is transferred to the host.

When the requested sectors have been verified, the device clears BSY and generates an interrupt.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the sector address of the sector where the error occurred. The Sector Count register shall contain the number of sectors not yet verified. The types of errors that are not retried when no retries is requested by the host is vendor specific.

ERRORS - Bad Block, Uncorrectable Data Error, ID Not Found Command Abort and Address Mark Not Found.

8.21. RECALIBRATE

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - None.

OUTPUTS - If the command is executed in CHS addressing mode, Cylinder High, Cylinder Low and the head portion of Device/Head shall be zero. The Sector Number register shall be 1. If the command is executed in LBA addressing mode, the Cylinder High, Cylinder Low, the head portion of the Device/Head and the Sector Number register shall be zero.

PREREQUISITES - None.

DESCRIPTION - This command moves the read/write heads to cylinder 0. Upon receipt of the command, the device sets BSY and performs a seek operation to cylinder zero. The device then waits for the seek to complete before updating status, clearing BSY and generating an interrupt.

Devices that implement power management may not perform the seek operation if the current power state is Idle or Standby. ERRORS - If the device cannot reach cylinder 0, a Track 0 Not Found error is posted.

8.22. SEEK

TYPE - Manadatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder High, Cylinder Low, head portion of the Device/Head register and the Sector Number register contain the logical sector number in CHS or LBA mode to which the device should move the read/write heads.

OUTPUTS - Same as the input registers.

PREREQUISITES - None.

DESCRIPTION - This command initiates a seek operation to the physical cylinder and head that contains the target logcial sector. If the device supports the indication of seek in progress and seek complete by clearing and setting the DSC bit in the Status register, then the device shall set DSC=0 when the seek operation is started and shall not set DSC=1 until the seek operation has completed. The device may clear BSY and generate an interrupt before the seek is completed.

Devices that implement power management may not perform the seek operation if the current power state is Idle or Standby. If another command is issued to the device while BSY=0 but DSC=1, the device sets BSY=1, waits for the seek to complete, and then begins execution of the command.

ERRORS - ID Not Found and Command Abort.

8.23. SET FEATURES

TYPE - Optional.

```
############################################################
#
#Hale's note:  Oh, come on now, we all know that Set Features
#really isn't optional any more!
#
############################################################
```

PROTOCOL - Non-data.

INPUTS - The Feature register contains a subcommand code as described in table 14. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

OUTPUTS - See the subcommand descriptions.

PREREQUISITES - None.

DESCRIPTION - This command is used by the host to establish the following parameters which affect the execution of certain device features as shown in table 14.

01h	Enable 8-bit data transfers (see 6.2.5)
02h	Enable write cache *
03h	Set transfer mode based on value in Sector Count register
33h	Disable retry *

44h	Length of vendor specific bytes on READ LONG/WRITE LONG cmds
54h	Set cache segments to Sector Count register value *
55h	Disable read look-ahead feature
66h	Disable reverting to power on defaults (see 8.23)
77h	Disable ECC *
81h	Disable 8-bit data transfers (see 6.2.5)
82h	Disable write cache *
88h	Enable ECC *
99h	Enable retries *
AAh	Enable read look-ahead feature
ABh	Set maximum prefetch using Sector Count register value *
BBh	4 bytes of vendor specific byts on READ LONG/WRITE LONG cmds
CCh	Enable reverting to power on defaults (see 8.23)
	*These feature definitions are vendor specific

1.1.1.1.1.1.1.1.5 Table 14 - Set Features register Definitions

All values not contained in Table 14 are reserved for future definition.

At power on, or after a hardware reset, the default mode is the same as that represented by values greater than 80h. A setting of 66h allows settings of greater than 80h which may have been modified since power on to remain at the same setting after a software reset.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000 000
PIO Default Transfer Mode, Disable IORDY	00000 001
PIO Flow Control Transfer Mode x	00001 nnn
Single Word DMA Mode x	00010 nnn
Multiword DMA Mode x	00100 nnn
Reserved	01000 nnn

where “nnn” is a valid mode number for the associated transfer type.

(Editor’s note: It is intended that the reserved values be used for future specification of an alternative flow control mechanism.)

If a device supports this specification, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000 000”, it shall set its default PIO transfer mode. If the value is “00000 001” and the device supports disabling of IORDY, then the device shall set its default PIO transfer mode and disable IORDY.

See vendor specification for the default mode of the commands which are vendor specific.

Devices reporting support for Multi Word DMA Transfer Mode 1 must also support Multi Word DMA Transfer Mode 0. Support of IORDY is mandatory when PIO Mode 3 is the current mode of operation.

ERRORS - If the device does not support the command or if any input value is is not supported or is invalid, the device posts an Aborted Command error.

8.24. SET MULTIPLE MODE

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - The Sector Count register contains number of sectors per block to use on all following READ/WRITE MULTIPLE commands. OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command enables the device to perform READ AND WRITE MULTIPLE operations and establishes the block count for these commands.

The Sector Count register is loaded with the number of sectors per block. Devices shall support block sizes of 2, 4, 8, and 16 sectors, if their buffer size is at least 8,192 bytes, and may also support other block sizes. Upon

receipt of the command, the device sets BSY=1 and checks the Sector Count register. If the Sector Count register contains a valid value and the block count is supported, the value is loaded for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and execution of those commands is enabled.

If the Sector Count register contains 0 when the command is issued, READ AND WRITE MULTIPLE commands are disabled.

At power on, or after a hardware reset, the default mode is READ AND WRITE MULTIPLE disabled. If Disable Default has been set in the Features register then the mode remains the same as that last established prior to a software reset, otherwise it reverts to the default of disabled.

ERRORS - If the device does not support the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands or if a block count is not supported, an Aborted Command error is posted, and READ MULTIPLE and WRITE MULTIPLE commands are disabled.

8.25. SLEEP

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command is the only way to cause the device to enter Sleep Mode.

This command causes the device to set BSY, prepare to enter Sleep mode, clear BSY and assert INTRQ. The host shall read the Status register in order to clear the interrupt and allow the device to enter Sleep mode. In Sleep mode the interface becomes inactive. The host shall not attempt to access the Command Block registers while the device is in Sleep mode.

Because some host systems may not read the Status register and clear the interrupt, a device may automatically deassert INTRQ and enter Sleep mode after a vendor specified time period of not less than 2 seconds.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

A device shall not power on in Sleep Mode nor remain in Sleep Mode following a reset sequence.

ERRORS - Command Abort - The device does not support the Power Management command set.

8.26. STANDBY

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby Timer. See Table ??.

Sector Count Register contents	Corresponding Timeout Period
0 (00h)	Timeout Disabled
1 - 240 (01h-F0h)	(value * 5) seconds
241 - 251 (F1h-FBh)	((value - 240) * 30) minutes
252 (FCh)	21 minutes
253 (FDh)	Vendor unique period between 8 and 12 hours
254 (FEh)	Reserved
255 (FFh)	21 minutes 15 seconds

1.1.1.1.1.1.1.1.6 Table ?? - Automatic Standby Timer Periods

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set BSY, enter the Standby Mode, clear BSY, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

ERRORS - Command Abort if the device does not support the Power

Management command set.

8.27. STANDBY IMMEDIATE

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set BSY, enter the Standby Mode, clear BSY, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

ERRORS - Command Abort - The device does not support the Power Management command set.

8.28. WRITE BUFFER

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - None.

OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to overwrite the contents of one sector in the the device's sector buffer When this command is issued, the device sets BSY, sets up the sector buffer for a write operation, sets DRQ, clears BSY, and waits for the host to write 512 bytes of data. Once the host has written the data, the device sets BSY, save the buffer data, clears BSY and generates an interrupt.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.
ERRORS - Command Abort if the command is not supported.

8.29. WRITE DMA

TYPE - Optional.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred or the address of the sector where the first error was detected.

PREREQUISITES - The host must initialize a slave-DMA channel.

DESCRIPTION - This command executes in a similar manner to WRITE SECTOR(S) except for the following:

- the host initializes a slave-DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write DMA command, the device shall provide status of BSY or DRQ until the command is completed. At command completion, the Command Block Registers contain the sector address of the last sector transferred.

An unrecoverable error encountered during the execution of a Write DMA command results in the termination of the command. At command completion, the Command Block Registers contain the sector address of the sector address of the sector where the first error occurred.

ERRORS - Command Abort if the command is not supported. Other errors possible are Bad Block, Uncorrectable data error, ID Not Found and Address Mark Not Found.

8.30. WRITE LONG

TYPE - Manadatory.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be written. The Sector Count register shall not specify a value other than 1.

OUTPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred or the address of the sector where the first error was detected.

PREREQUISITES - The SET FEATURES subcommand to enable more than 4 vendor specific bytes must be executed prior to the WRITE LONG command if more than 4 vendor specific bytes are to be transferred.
DESCRIPTION - This command is similar to the WRITE SECTOR(S) command except that it writes the data and the vendor specific bytes as supplied by the host; the device does not generate the vendor specific bytes itself. Only single sector Write Long operations are supported.

The transfer of the vendor specific bytes shall be one byte at a time over bits DD0-7 only (8-bits wide).

ERRORS - Bad Block, ID Not Found Command Abort and Address Mark Not Found.

8.31. WRITE MULTIPLE command

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - If not error, the Cylinder Low, Cylinder High,

Device/Head and Sector Number registers specify the address of the last sector transferred. These registers are undefined if an error condition is indicated at command completion.

PREREQUISITES - A successful SET MULTIPLE MODE command must preceed a READ MULTIPLE command.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command. interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by SET MULTIPLE MODE.

Command execution is identical to the WRITE SECTOR(S) operation except that the number of sectors defined by the SET MULTIPLE MODE command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where n = Remainder (SECTOR COUNT / block count)

If the WRITE MULTIPLE command is attempted before the SET MULTIPLE MODE command has been executed or when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with an Aborted Command error.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The Write command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

ERRORS - Bad Block, Uncorrectable Data Error, ID Not Found Command Abort and Address Mark Not Found.

8.32. WRITE SAME

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Feature register contains a sub command code, either 22H or DDH. If the Feature register contains 22H, the Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be written. The Sector Count register specifies the number of sectors to be written (not the number of sectors transferred by the host). If the Feature register contains code DDH, the Cylinder High, Cylinder Low, head portion of the Device/Head, Sector Number and Sector Count registers are not used.

OUTPUTS - If no error, the Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector written. If the comamnd ends with an error, these registers contain the address of the sector where the first error was detected and the Sector Count register contains the number of sectors remaining to be transferred in order to complete the original request.

PREREQUISITES - None.

DESCRIPTION - This command executes in a similar manner to WRITE SECTOR(S) except that only one sector of data is transferred. The contents of the sector are written to the media one or more times.

> NOTE: The WRITE SAME command allows for initialization of part or all of the medium to the specified data with a single command. If the Features register is 22h, the device shall write that part of the medium specified by the Sector Count, Sector Number, Cylinder Low, Cylinder High and Device/Head registers. If the Features register contains DDh, the device shall initialize all the user accessible medium.

The device issues an interrupt to indicate that the command is complete. Any error encountered during execution results in the termination of the write operation.

ERRORS - If the Feature register contains a value other than 22h or DDh, the command shall be rejected with an aborted command error. Other errors possible are Bad Block, Uncorrectable Data Error, ID Not Found and Address Mark Not Found.

8.33. WRITE SECTOR(S)

TYPE - Manadatory.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - If no error, the Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred. If the comamnd ends with an error, these registers contain the address of the sector where the first error was detected and the Sector Count register contains the number of sectors remaining to be transferred in order to complete the original request.

PREREQUISITES - None.

DESCRIPTION - This command writes from 1 to 256 sectors as specified in the Sector Count register. A SECTOR COUNT of 0 requests 256 sectors. If the device is not already on the desired track, an implied seek

operation is performed. The types of errors that are not retried when no retries is requested by the host is vendor specific.

ERRORS - Bad Block, Uncorrectable Data Error, ID Not Found Command Abort and Address Mark Not Found.

8.34. WRITE VERIFY

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the the starting CHS or LBA sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

OUTPUTS - If no error, the Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the address of the last sector transferred. If the comamnd ends with an error, these registers contain the address of the sector where the first error was detected and the Sector Count register contains the number of sectors remaining to be transferred in order to complete the original request.

PREREQUISITES - None.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command, except that each sector is verified immediately after being written. The verify operation is a read without transfer and a check for data errors. Any errors encountered during the verify operation are posted. Multiple sector WRITE VERIFY commands write all the requested sectors and then verify all the requested sectors before generating the final interrupt.

ERRORS - Bad Block, Uncorrectable Data Error, ID Not Found Command Abort and Address Mark Not Found.

Well, this is just about it. The control of your email will be returned to you shortly after receiving this messsage! I'm sure many of you are happy to heard this news.

Here is the latest version of Annexes A and B. These Annexes have been under discussion for awhile now and the previous version of this message, 94-065-r2 dated 24 April 94, is what you will find in the ATA-2 Rev 2F document.

Master/Slave Handshaking

Document 94-065-r3

25 August 94

by Hale Landis

This is a major revision since 94-065-r2 (and ATA-2 rev 2f). I have been trying to make this whole mess easy to understand. I hope I have done that with this version. I also added the recommendation that a host allow up to 2 minutes for DRDY=1 based on the discussion started by Conner at our previous meetings. I suggest that you review this carefully—it is relatively complex and I could have make a mistake (yep, it can happen).

Annex A Diagnostic and reset considerations from a device hardware standpoint (informative)

This annex describes the algorithm and timing relationships for devices 0 and 1 during the processing of power on and hardware resets, software resets, and the EXECUTE DEVICE DIAGNOSTIC command.

The timing assumes the following:

a) DASP- is asserted by Device 1 and received by Device 0 at power-on or hardware reset to indicate the presence of Device 1. At all other times it is asserted by Device 0 or Device 1 to indicate when a device is active.
b) PDIAG- is asserted by Device 1 and detected by Device 0. It is used by Device 1 to indicate to Device 0 that it has completed diagnostics and is ready to accept commands from the Host (BSY bit is cleared). This does not indicate that the device is ready, only that it can accept commands. This line may remain asserted until the next reset occurs or an EXECUTE DEVICE DIAGNOSTIC command is received.

A.1 Power on and hardware resets

A.1.1 Power on and hardware resets - device 0

a) Host asserts RESET- for a minimum of 25 usec.
b) Device 0 sets BSY within 400 nsec after RESET- is negated.
c) Device 0 negates DASP- within 1 msec after RESET- is negated.
d) Device 0 samples for at least 450 msec for DASP- to be asserted from Device 1. This sampling starts 1 ms after RESET-is negated.
e) Device 0 performs hardware initialization and diagnostics.
f) Device 0 may revert to its default condition.
g) If Device 0 detected that DASP- was asserted during step d), then Device 0 waits up to 31 seconds for Device 1 to assert PDIAG-. If PDIAG- is asserted within 31 seconds, Device 0 sets bit 7=0 in the Error Register, else Device 0 sets bit 7=1 in the Error Register.

If DASP- assertion was not detected in step d), Device 0 sets bit 7=0 in the Error Register.

NOTE: Device 0 must remember if Device 1 was detected in step d) because this information is need in order to process any Software reset or EXECUTE DEVICE DIAGNOSTIC command later.

h) Device 0 posts diagnostic results to bits 6-0 of the Error Register.
i) Device 0 clears BSY when ready to accept commands that do not require DRDY=1.

NOTE: Device 0 must clear BSY within 31 seconds from the time that RESET- is negated.

j) Device 0 sets DRDY when ready to accept any command.

NOTE: Steps i) and j) may occur at the same time. While no maximum time is specified for DRDY=1 to occur a host is advised to allow up to 2 minutes for DRDY=1. See Figure 9.

A.1.2 Power on and hardware resets - device 1

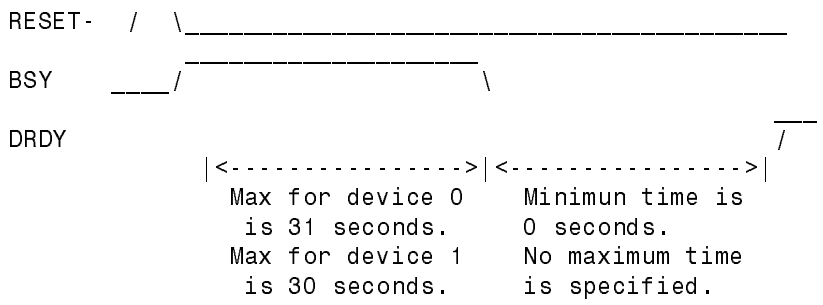
a) Host asserts RESET- for a minimum of 25 usec.
b) Device 1 sets BSY within 400 nsec after RESET- is negated.
c) Device 1 negates DASP- within 1 msec after RESET- is negated.
d) Device 1 negates PDIAG- before asserting DASP-.
e) Device 1 asserts DASP- within 400 msecs after RESET- is negated.
f) Device 1 performs hardware initialization and diagnostics.
g) Device 1 may revert to its default condition.
h) Device 1 posts diagnostic results to the Error Register.
i) Device 1 clears BSY when ready to accept commands that do not require DRDY=1.
j) If Device 1 passed its diagnostics without error in step f), Device 1 asserts PDIAG-. If those diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step.

NOTE: Device 1 must clear BSY, and optionally assert PDIAG-, within 30 seconds from the time RESET- is negated.

k) Device 1 sets DRDY when ready to accept any command.

NOTE: Steps i), j) and k) may occur at the same time. While no maximum time is specified for DRDY=1 to occur, a host is advised to allow up to 2 minutes for DRDY=1. See Figure 9.

l) Device 1 negates DASP- after the first command is received or negates DASP- if no command is received within 31 seconds after RESET- is asserted.



1.1.1.1.1.1.2 Figure 9- BSY and DRDY timing for power on and hardware resets

A.2 Software reset

A.2.1 Software reset - device 0

a) Host sets SRST=1 in the Device Control register.
b) Device 0 sets BSY within 400 nsec after detecting that SRST=1.
c) Device 0 performs hardware initialization and diagnostics.
d) Device 0 may revert to its default condition.
e) Device 0 posts diagnostic results to the Error Register.
f) Device 0 waits for the host to set SRST=0.
g) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 31 seconds from the time that SRST=0 for Device 1 to assert PDIAG-. If PDIAG- is asserted within 31 seconds, Device 0 sets bit 7=0 in the Error Register, else Device 0 sets bit 7=1 in the Error Register. If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 sets bit 7=0 in the Error register.
h) Device 0 clears BSY when ready to accept commands that do not require DRDY=1.

NOTE: Device 0 must clear BSY within 31 seconds from the time that the host sets SRST=0.

i) Device 0 sets DRDY when ready to accept any command.

NOTE: Steps h) and i) may occur at the same time. While no maximum time is specified for DRDY=1 to occur, a host is advised to allow up to 2 minutes for DRDY=1. See Figure 10.

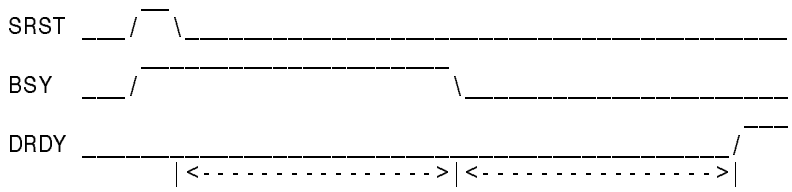
A.2.2 Software reset - device 1

a) Host sets SRST=1 in the Device Control register.
b) Device 1 set BSY within 400 nsec after detecting that SRST=1.
c) Device 1 negates PDIAG- within 1 msec after detecting that SRST=1.
d) Device 1 perform hardware initialization and diagnostics.
e) Device 1 may revert to its default condition.
f) Device 1 posts diagnostic results to the Error Register.
g) Device 1 waits for the host to set SRST=0.
h) Device 1 clears BSY when ready to accept commands that do not require DRDY=1.
i) If Device 1 passed its diagnostics without error in step d), Device 1 asserts PDIAG-. If those diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step.

NOTE: Device 1 must clear BSY, optionally assert PDIAG-, within 30 seconds from the time the host sets SRST=0.

j) Device 1 sets DRDY when ready to accept any command.

NOTE: Steps h), i) and j) may occur at the same time. While no maximum time is specified for DRDY=1 to occur, a host is advised to allow up to 2 minutes for DRDY=1. See Figure 10.



```
Max for device 0    Minimun time is
 is 31 seconds.     0 seconds.
Max for device 1    No maximum time
 is 30 seconds.     is specified.
```

1.1.1.1.1.1.3 Figure 10- BSY and DRDY timing for software reset

A.3 EXECUTE DEVICE DIAGNOSTIC Command Execution

A.3.1 EXECUTE DEVICE DIAGNOSTIC command execution - device 0

a) Device 0 sets BSY within 400 nsec after the EXECUTE DEVICE DIAGNOSTIC command is received.
b) Device 0 performs hardware initialization and diagnostics.
c) Device 0 resets the Command Block registers to default condition.
d) Device 0 posts diagnostic results to bits 6-0 of the Error Register.
e) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 6 seconds from the time that the EXECUTE DEVICE DIAGNOSTIC command was received for Device 1 to assert PDIAG-. If PDIAG- is asserted within 6 seconds, Device 0 sets bit 7=0 in the Error Register, else Device 0 sets bit 7=1 in the Error Register.
If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 sets bit 7=0 in the Error register.
f) Device 0 clears BSY when ready to accept commands that do not require DRDY=1.

NOTE: Device 0 must clear BSY within 6 seconds from the time that the EXECUTE DEVICE DIAGNOSTIC command was received.

g) Device 0 sets DRDY when ready to accept any command.

NOTE: Steps f) and g) may occur at the same time. While no maximum time is specified for DRDY=1 to occur, a host is advised to allow up to 2 minutes for DRDY=1. See Figure 11.

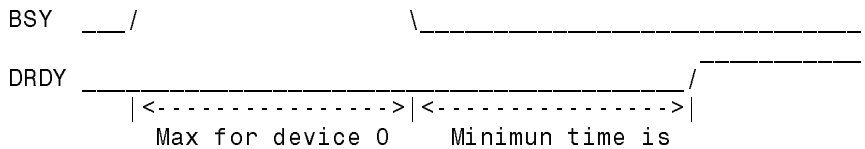
A.3.2 EXECUTE DEVICE DIAGNOSTIC command execution - device 1

a) Device 1 sets BSY within 400 nsec after the EXECUTE DEVICE DIAGNOSTIC command is received.
b) Device 1 negates PDIAG- within 1 msec after the command received.
c) Device 1 performs hardware initialization and diagnostics.
d) Device 1 resets the Command Block registers to the default condition.
e) Device 1 posts diagnostic results to the Error Register.
f) Device 1 clears BSY when ready to accept commands that do not require DRDY=1.
g) If Device 1 passed its diagnostics without error in step c), Device 1 asserts PDIAG-. If those diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step.

NOTE: Device 1 must clear BSY and assert PDIAG- within 5 seconds from the time RESET- is asserted.

h) Device 1 sets DRDY when ready to accept any command.

NOTE: Steps f), g) and h) may occur at the same time. While no maximum time is specified for DRDY=1 to occur, a host is advised to allow up to 2 minutes for DRDY=1. See Figure 11.




```
Max for device 0    Minimun time is
 is  6 seconds.     0 seconds.
Max for device 1    No maximum time
 is  5 seconds.     is specified.
```

2. Figure 11- BSY and DRDY timing for Diagnostic command

Annex B. Diagnostic and reset considerations from a device firmware standpoint (informative)

B.1. Power on and hardware reset (RESET-)

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 will read PDIAG- to determine when it is valid to clear BSY and whether Device 1 has powered on or reset without error, otherwise Device 0 clears BSY whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity.

B.2. Software reset

If Device 1 is present Device 0 will read PDIAG- to determine when it is valid to clear BSY and whether Device 1 has reset without any errors, otherwise Device 0 will simply reset and clear BSY. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

B.3. Device diagnostic command

If Device 1 is present, Device 0 will read PDIAG- to determine when it is valid to clear BSY and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command, otherwise Device 0 will simply execute its diagnostics and then clear BSY. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

B.4. Truth table

In all the above cases: Power on, RESET-, software reset, and the EXECUTE DEVICE DIAGNOSTIC command the Device 0 Error register is calculated as follows:

Device 1 Present?	PDIAG- Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

Where x indicates the appropriate Diagnostic Code for the Power on, RESET-, software reset, or device diagnostics error.

2.1.1.1.1.1.1.1 Table 14 - Reset Error register Values

B.5. Power on or hardware reset algorithm

NOTE: In the following algrorithms, the notation 1* refers to the Drive 1 status register copy that Drive 0 keeps when there is no Drive 1 present.

B.5.1. Algorithm for Device 0

1) Power on or hardware reset is detected by the device's hardware.
2) The hardware should automatically do the following within 400 nsec:
   a) Set up the hardware to report both Device 0 and Device 1* status registers.
   b) Set the Device 0 Status register to 80h.
   c) Set the Device 1* Status register to 80h.
3) The device must determine if it is Device 0 or Device 1. This can be done at least two different ways: by jumper or by using the CSEL signal. This algorithm is for Device 0.
4) Set up PDIAG- and DASP:
   a) Set up PDIAG- as an input.
   b) Release DASP- and set up DASP- as an input.
   c) Monitor DASP- for 450 msec or until DASP- is asserted by Device 1.
   d) If DASP- is asserted within 450 msec, note that Device 1 is present and set up the hardware so it reports Device 0 status only and remember the Device 1 is present.

e) If DASP- is not asserted within 450 msec, note that Device 1 is not present and set up the hardware so it reports both Device 0 and 1* status registers and remember that Device 1 is not present.
f) Set up DASP- as an output.
g) Assert DASP-.

NOTE: Steps 1-4 must complete within 450 msec.

5) Perform any remaining time critical hardware initialization including starting the spin up of the device if needed. Complete all the hardware initialization and diagnostic tests needed to get the device ready, including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
6) If Device 1 was detected in step 4:
   a) Monitor PDIAG- for 31 seconds or until PDIAG- is asserted by Device 1.
   b) If PDIAG- is asserted within 31 seconds, set bit 7=0 in the Error register.
   c) If PDIAG- is not asserted within 31 seconds, set bit 7=1 in the Error register.
7) Post Device 0's initialization and diagnostic results:
   a) If Device 0 completed all initialization and diagnostics without error, set bits 6-0 of the Error register to 1.
   b) If Device 0 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value of 2 or greater indicating the type of failure.
8) Set the status register to 00h and set Drive 1* Status register to 00H.

NOTE: Steps 1-8 must complete within 31 seconds.

9) Finish initialization and optionally finish spin up.
10) Post Ready status:
    a) Set the Status register to 40h or if spin up is complete set the status register to 50h.
    b) Negate DASP-
11) If not previously done, wait for spin up to complete and then set the status register to 50h.

B.5.2. Algorithm for Device 1

1) Power on or hardware reset is detected by the device's hardware.
2) The hardware should automatically do the following within 400 nsec:
   a) Set up the hardware to report both Device 0 and Device 1* status registers.
   b) Set the Device 0 Status register to 80h.
   c) Set the Device 1* Status register to 80h.
3) The device must determine if it is Device 0 or Device 1. This can be done at least two different ways: by jumper or by using the CSEL signal. This algorithm is for Device 1.
4) Set up PDIAG- and DASP:
   a) Negate the PDIAG- signal.
   b) Set up PDIAG- as an output.
   c) Assert the DASP- output.
   d) Set up DASP- as an output.
   e) Set up the hardware so it reports Device 1 status only.

NOTE: Steps 1-4 must complete within 400 msec.

5) Perform any remaining time critical hardware initialization including starting the spin up of the device if needed. Complete all the hardware initialization and diagnostic tests needed to get the device ready, including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
6) Post Device 1's initialization and diagnostic results:
   a) If Device 1 completed all initialization and diagnostic without error, Set the Error register to 1 and assert PDIAG-.
   b) If Device 1 failed any initialization or diagnostics, set the Error register to a value of 2 or greater indicating the type of failure and do not assert PDIAG-.

7) Set the status register to 00.

NOTE: Steps 1-7 must complete within 30 seconds.

8) Finish initialization and optionally finish spin up.
9) Post Ready status: Set the Status register to 40h or if spin up is also complete set the Status register to 50h.
10) If not previously done, wait for spin up to complete and then set the status register to 50h.
11) Negate DASP- when the Command register is written or after 31 seconds.

B.6 Software Reset Algorithm

B.6.1 Algorithm for Device 0

1) SRST=1 is detected by the device's hardware.
2) The hardware should set 80h in the Status register within 400 nsec.
3) If there is no Device 1, the hardware should set the Device 1* Status register to 80h

NOTE: Steps 1-3 must happen within 1 msec.

4) Assert DASP-.
5) Finish all the hardware initialization needed to place the device in reset including all diagnostics.
6) Wait for SRST=0.
7) Reset the Command Block registers:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
8) If Device 1 is present:
   a) Monitor PDIAG- for 31 seconds or until PDIAG- is asserted by Device 1.
   b) If PDIAG- is asserted within 31 seconds, set bit 7=0 in the Error register.
   c) If PDIAG- is not asserted within 31 seconds, set bit 7=1 in the Error register.
9) Post Device 0's initialization and diagnostic results:
   a) If Device 0 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 1.
   b) If Device 0 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value of 2 or greater indicating the type of failure.

NOTE: Steps 7-9 must complete within 31 seconds.

10) Set the Status register to 50h and set Drive 1* Status register to 00h.

B.6.2 Algorithm for Device 1

1) SRST=1 is detected by the device's hardware.
2) The hardware should set 80h in the Status register within 400 nsec.
3) Negate the PDIAG- signal.

NOTE: Steps 1-3 must complete within 1 msec.

4) Assert DASP-.
5) Finish all the hardware initialization needed to place the device in reset including all diagnostics.
6) Wait for SRST=0.
7) Reset the Command Block registers:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
8) Post Device 1's initialization and diagnostic results:
   a) If Device 1 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 1and assert PDIAG-.
   b) If Device 1 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value of 2 or greater indicating the type of failure and do not assert PDIAG-.

NOTE: Steps 7-9 must complete within 30 seconds.

9) Set the Status register to 50h.

B.7. EXECUTE DEVICE DIAGNOSTIC Command Algorithm

B.7.1. Algorithm for Device 0

1) The EXECUTE DEVICE DIAGNOSTIC command is received.
2) The hardware should set 80h in the Status register within 400 nsec.
3) The hardware should set 80h in the Device 1* Status register.

NOTE: Steps 1-3 must complete within 1 msec.

4) Assert DASP-.
5) Perform all the device diagnostics and note the results.
6) Finish all the hardware initialization needed to get the device ready to receive any type of command from the host including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
7) If Device 1 is present:
   a) Monitor PDIAG- for 6 seconds or until PDIAG- is asserted by Device 1.
   b) If PDIAG- is asserted within 6 seconds, set bit 7=0 in the Error register.
   c) If PDIAG- is not asserted within 6 seconds, set bit 7=1 in the Error register.
8) Post Device 0's initialization and diagnostic results:
   a) If Device 0 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 1.
   b) If Device 0 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value of 2 or greater indicating the type of failure.

NOTE: Steps 1-8 must complete within 6 seconds.

9) Set the Status register to 50h and set Drive 1* Status register to 00h.
10) Assert INTRQ.

B.7.2. Algorithm for Device 1

1) The EXECUTE DEVICE DIAGNOSTIC command is received.
2) The hardware should set 80h in the Status register within 400 nsec.
3) Negate the PDIAG- signal.

NOTE: Steps 1-3 must complete within 1 msec.

4) Assert DASP-.
5) Perform all the device diagnostics and note the results.
6) Finish all the hardware initialization needed to get the device ready to receive any type of command from the host including:
   a) Set the Sector Count register to 01h.
   b) Set the Sector Number register to 01h.
   c) Set the Cylinder Low register to 00h.
   d) Set the Cylinder High register to 00h.
   e) Set the Device/Head register to 00h.
7) Post Device 1's initialization and diagnostic results:
   a) If Device 1 completed all initialization and diagnostics without error, set bits 6-0 of the Error register the value 1and assert PDIAG-.
   b) If Device 1 failed any initialization or diagnostics, set bits 6-0 of the Error register to a value of 2 or greater indicating the type of failure and do not assert PDIAG-.

NOTE: Steps 1-7 must complete within 5 seconds.

8) Set the Status register to 50h.