TO: **John Lohmeyer, Chairman, X3T10 Committee (SCSI)**

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IEEE P1285 Liaison to X3T10/DADI

Date: **July 15, 1994**

Subject: **P1285 Liaison Report for July 1994**

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o Two interface levels: Beta & Gamma
- o Beta Level: One controller, multiple slaves
- o Gamma Level: Multiple masters
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Self-synchronous data transfer
- o Live insertion / removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

There were numerous discussions about topics not yet covered in the P1285 draft document. A new operational view of the gamma level
interface was discussed, and a new mechanism known as a "streamer" was devised. A streamer is the data structure and control for a new form of data transfer unit. It

provides the capability for self-synchronous data transfers --- where I/O stream synchronization may be controlled by device commands and not need interaction with the system software. This make data transfers more efficient. A device may have one or more streamers. The group is looking into extending this concept to the beta level.

A major topic concerned how devices are initialized and which register sets the system has access to at which time. For instance, a PCI device first needs initialization so that its CSR registers can be accessed directly, then the P1285 CSR registers need initialization followed by the device-specific registers.

Hot-swapping PCI was discussed. A hot-swapping logical level protocol will be added to P1285. It is up to the PCI working group to specify the electrical and mechanical aspects.

The group discussed additional support for RAID configurations.
Currently, there is an EXOR command that can be used at the beta and gamma levels to aid in RAID parity calculations. The idea was to try to support RAID data reconstruction mode by distributed processing in the associated devices rather than in a separate disk array controller or in system software.

Upcoming Events

Future meetings are scheduled as follows:

* July	19	Co-located Meeting with X3T10, Manchester, NH.
August	17	Apple Computer, 1 Infinite Loop, Cupertino, CA.

Meetings are usually scheduled from 2:00-5:00 PM.

* Co-located Meeting with X3T10 scheduled from 5:00-8:00 PM.