Accredited Standards Committee*
X3, Information Processing Systems

Doc. No. X3T10/94-131R0
Date: June 2, 1994
Project:
Ref. Doc.:
Reply to: J. Lohmeyer

To: Membership of X3T10

From: Lamers/Lohmeyer

Subject: Minutes of X3T10 FAST-20 Study Group June 2, 1994

Agenda

Results of Meeting

1. Opening Remarks

John Lohmeyer convened the meeting at 9:30 am. John thanked Jim McGrath of Quantum for hosting the meeting.

As is customary, the people attending introduced themselves. A copy of the attendance list was circulated for attendance and corrections.

It was stated that the meeting had been authorized by X3T10 and would be conducted under the X3 rules. Ad hoc meetings take no final actions, but prepare recommendations for approval by the X3T10 task group. The voting rules for the meeting are those of the parent committee, X3T10. These rules are: one vote per company; and any participating company member may vote.

The minutes of this meeting will be posted to the SCSI BBS and the SCSI Reflector and will be included in the next committee mailing.

2. Attendance and Membership, Introductions

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or company to attend and to express their opinion on the subjects being discussed.

The following people attended the meeting.

Attendee	Company	Email Address
Lawrence J. Lamers	Adaptec	ljlamers@aol.com
Norm Harris	Adaptec	nharris@adaptec.com
Wally Bridgewater	Adaptec	wally@eng.adaptec.com
Mark Knecht	AMD	mark.knecht@amd.com
David Wang	AMD	david.wang@amd.com
John Lohmeyer	AT&T/NCR Microelectronics	john.lohmeyer@ftcollinsco.ncr.com
Joe Stoupa	Burr-Brown Corp	
Dale Smith	Cirrus Logic	dale@cirrus.com
Louis Grantham	Dallas Semiconductor	
Bill Ham	Digital Equipment Corp	ham@subsys.enet.dec.com
Ting Chan	Qlogic	@qlc.com
Jim McGrath	Quantum Corp	jmcgrath@qntm.com
Jamse Oliver	Silicon Graphics	oliver@sgi.com
Vit Novak	Sun Microsystems	vit.novak@sun.com
Jack Shiao	Tandem Computer	shiao_jack@tandem.com
Pete Tobias	Tandem Computer	tobias_pete@tandem.com
Kevin Gingerich	Texas Instruements	
Paul Aloisi	Unitrode Integrated Circuit	aloisi@uicc.com

3. Approval of Agenda

The agenda was approved as proposed. Item 5.2.4, 5.2.5, and 5.3 were added during the meeting.

4. Document Distribution

X3T10/94-103r1 Proposed Implementor's Note for FAST-20 Node Capacitance

5. Old Business

5.1 Single-ended Update [94-xxx] (Ham)

Bill Ham presented his latest data on FAST-20 single-ended. The data showed that the propagation delay has a significant impact on being able to run at 20 MHz. Each load on the cable adds approximately 0.5 ns delay to the signal. Since single-ended is relying on reflections to get the amplitude up the propagation delays affects the ability to get a valid signal.

This assumes non-incident wave switching.

The model looks like an AC transmission line voltage divider. Reducing the number of loads or reducing the node capacitance improves the situation.

Number of devices
Node Capacitance
Cable Length

Reducing cable length reduces prop delay so reflections arrive in time to reduce the shelf.
The impedance mis-match between devices and cable is main problem.

It looks like a table showing the trade-offs of number of devices, cable length, and node capacitance.

Suggested to calculate distributed capacitance for adding devices as a function of load and spacing.

Bill Ham noted that given the test results it is likely that 16 devices on a 3 meter bus for FAST-10 has signal issues.

Wally noted that most of the threshold variation comes from power supply variations. He suggested a 0.5% tolerance on power supply. Mixed environments (slow and fast) can be a problem because of the low hysterisis in noisier environments. The consensus was 5.0% tolerance on power supply voltage. A temperature range of 0-70 degrees C.

Bill Ham reiterated the need for changing the thresholds. If the thresholds don't change some other parameter needs to be modified.

Kevin Gingerich stated that a minimum current for active negation also needs to be specified to assure that the first step to 2.0 volts is made in the face of a impedance mismatch at the middle of the cable. The calculation assumed a 3.24 high voltage, a 0.2 low voltage, a 20 ohm impedance mismatch on an 84 ohm impedance, maintaining the 0.8 volt step. This resulted in a 62 ma driver requirement which was then reduced by the current input from the active terminators. The result is a 22 ma minimum active negation strength driver is required at 2.0 v D.C.

Kevin Gingerich presented a formulae for calculating the allowed number of devices based on bus capacitance.
Z0=sq(L/C) assuming cable at 10 pf/ft.
Z0'= sq(L/(C+C'))
Z0'/Z0=sq(1/(1+C/C'))
C'/C=.75
C'=7.5 pf/ft
Kevin took an action item to draft this as an informative annex.

5.2 FAST-20 Specs [94-xxx] ()

5.2.1 Receiver Voltage Level

	proposed	consensus
vIHH	1.9	1.9
vIHL	1.6	1.6
vILH	1.4	1.3

vILL 1.1 1.0

5.2.2 Node Capacitance
20pf maximum, but lower is better

5.2.3 Cable Length
depends on number of devices - 1.5 meters for 8 devices; 3.0 meters for 3 devices

5.2.4 Number of Devices
depends on cable length - 8 devices at 1.5 meters; 3 devices at 3.0 meters

5.2.5 Minimum Strength of Active Negation
vOH (xx) = 2.0 v D.C> min 22 ma negation

5.3 Implementor's Note for FAST-20 [94-103r1] (Novak)
Accepted as modified.

6. New Business

6.1 Transfer Period [] (Lohmeyer)

How to specify the FAST-20 synchronous transfer rate. Because the transfer period is modulo 4 it is not possible to specify exactly 20 Mb/sec. What can be achieved is:

20.83 Mb/sec (48 ns period) with a value of 12
19.23 Mb/sec (52 ns period) with a value of 13

Add implementor's note to advise folks of this issue.

6.2 Voh Termination/Drivers [94-038r3] (Aloisi)

The current SPI document does not specify a maximum voltage in the terminator nor the driver. The consensus is to put in the limitation on the terminator sourcing current above 3.24 v D.C. The max Voh will be specified at 3.7 v D.C. max.

The correct approach is to specify the min Vih and leave the max Vih to the silicon vendor. The test circuit in the document is used to measure these voltages.

Leave of the 0.0 on Vil and specify 0.8 Vil max. The min Vil is specified by the vendor.

6.3 Differential Update [94-xxx] (Ham)

Bill Ham reported on the differential testing he has done. One recommendation is to specify a min of 2 volts. Drop Vod specification since RS-485 is more restrictive. Another is to draft more relaxed configuration rules.

Bill stated that differential works so well but has a power dissipation problem. He suggested that reduced voltage swings could allow on chip drivers and still offer headroom for higher transfer rates. On chip drivers reduce skew management issues. Kevin Gingerich stated that it is technically feasible but common mode will be reduced. 200 Mb/sec parallel SCSI is a definite possibility.

7. Meeting Schedule

No future meetings planned on FAST-20.

8. Adjournment

1. The meeting adjourned at 4:00 PM.