

Accredited Standards Committee*
X3, Information Processing Systems

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To: X3T10 Membership
Subject: Proposal for Control Mechanism for Reserved Handling

At the May 1994 X3T10 meeting, a motion to reverse the sense of the current reserved field checking requirements in SCSI-3 passed by a vote of 16:10. The voting margin was too close to believe that the action represents a real consensus on the topic. I believe that many of those in the minority on this action (including me) could be persuaded to join the majority if there were some explicit mechanism to control this behavior. Consequently, I propose that the section on "Reserved" be revised and a DRC bit be added to bit 3 of byte 4 in the Control Mode Page in SPC as follows:

x.x.x Reserved

Reserved bits, fields, bytes, and code values are set aside for future standardization. Their use and interpretation may be specified by future extensions to this standard. A reserved bit, field, or byte shall be set to zero, or in accordance with a future extension to this standard. A target that receives a reserved bit, field, or byte that is not zero or receives a reserved code value shall:

- a) If the DRC bit in the control mode page is one, the target shall ignore nonzero reserved bits, fields, and bytes. The target may, at its discretion, map reserved code values to supported code values or terminate the command with CHECK CONDITION status and a sense key of ILLEGAL REQUEST.
- b) If the DRC bit in the control mode page is zero, the target shall terminate the command with CHECK CONDITION status and a sense key of ILLEGAL REQUEST.

It shall also be acceptable for a target to interpret a bit, field, byte, or code value in accordance with a future extension to this standard.

* Operating under the procedures of The American National Standards Institute.

Control mode page								
Bit	7	6	5	4	3	2	1	0
Byte								
0	PS	Reserved		Page code (0Ah)				
1				Page length (06h)				
2				Reserved				RLEC
3	Queue algorithm modifier			Reserved			QErr	DQue
4	EECA	Reserved		DRC	RAENP	UAAENP	EAENP	
5				Reserved				
6	(MSB)				Ready AEN holdoff period			
7								(LSB)

A disable reserved checking (DRC) bit of one specifies that the target shall not perform checking of reserved bits, fields, and bytes. The target may perform checking of reserved code values or may map reserved code values into supported code values, at its discretion.

A DRC bit of zero specifies that the target shall perform checking of reserved bits, fields, bytes, and code values as described in x.x.x.