*Cirrus Logic*
3100 West Warren Avenue, Fremont, CA 94538, Tel. (510) 249-4953, Fax (510) 249-4940

**DATE:** 5-17-94

**TO:** X3T10 ATA working group

**FROM:** John Geldman

**SUBJECT:** 0948dr2.doc comments

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These are the comments I have so far from my review of this document.
See you in Harrisburg.

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Section 3.1.1, page 13

With two additional connectors in the annex, the type of connector should not be emphasized.

Was:
ATA defines a register set, a 40-pin connector and the associated signals on the connector.

Suggested:
ATA defines a register, command, and protocol set, along with connector and signal definitions.

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Section 3.2.5, page 16

The byte order described here is not essential, as all drives tend to deliver data back in the order it was received. However, the typical Intel orientation that ATA started with would have had the high byte of word (x).

Was:

```
DD DD DD DD DD DD DD DD   DD DD DD DD DD DD DD DD
        15 14 13 12 11 10 09 08   07 06 05 04 03 02 01 00
Word(x)    --------Byte(0)--------   --------Byte(1)--------
Word(x+1)  --------Byte(2)--------   --------Byte(3)--------
```

Suggested:

```
DD DD DD DD DD DD DD DD   DD DD DD DD DD DD DD DD
        15 14 13 12 11 10 09 08   07 06 05 04 03 02 01 00
Word(x)    --------Byte(1)--------   --------Byte(0)--------
Word(x+1)  --------Byte(3)--------   --------Byte(2)--------
```

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Section 4, page 17:

The editor asked for suggestions on how to define legal connections and cabling configurations. One suggestion is to allow only one piece and type of cable (to avoid SCSI-type impedance mis-match reflections), however any connector-based coupler (68 pin drive to 44 pin cable) would be legal.

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Section 4.2.2, page 19 Section 4.6, page 21

My notes show that on February 23rd, the Working Group agreed to remove all references to 3.3V systems as we had not provided a complete specification for operating at this power level.

Was:

| Power Line Designation | | Pin Number |
|---|---|---|
| +5 Volts | +3.3 Volts | 1 |
| +12 Volts | +5 Volts | 2 |
| Ground | Ground | 3 |

Table 2 - DC Interface Using 3 Pin Power Connector
**Error! Bookmark not defined.**

[Editor's Note: How do we specify the pin one orientation?]

A drive designed for 3,3V applications may be plugged into a receptacle designed to accept a drive designed for 5V applications, with 12V lines for additional power. It is not required that the drive operate, but it is recommended that precautions be taken to prevent damage to the drive.

A drive designed for 5V applications may be plugged into a receptacle designed to accept a drive designed for 3,3V applications, with 5V lines for additional power. It is not anticipated that damage could occur to the drive, but it is likely to fail in an undetermined manner.

Suggested:

| Power Line Designation | Pin Number |
|---|---|
| +5 Volts | 1 |
| +12 Volts | 2 |
| Ground | 3 |

Table 2 - DC Interface Using 3 Pin Power Connector

[Editor's Note: How do we specify the pin one orientation?]

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Section 4.6, page 21

First, similar to the previous comment, the working group has agreed to remove references to 3.3V. This would include the entries specific to 3.3V and the comments differentiating the 5.0V specifications.

Second, a suggestion for rise and fall (which I had been asked to write). The key concern was when discussing a percentage of full amplitude, just what is full amplitude. The suggested text refers to a relatively slow signal into a well-behaved test circuit. There should not be any significant overshoot or undershoot problems.

Was:

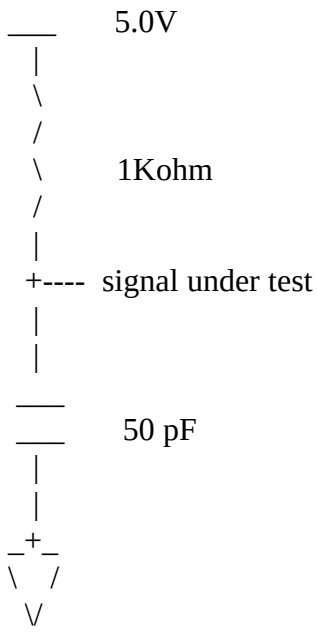
| tRISE | Rise time for any signal on AT interface(1)| 5ns | |
|---|---|---|---|
| tFALL | Rise time for any signal on AT interface(1)| 5ns | |

(1) tRISE and tFALL are measured from 0.5V to 2.8V with a resistive load of 1k ohm and a capacitive load of 50 pF.

Suggested:

| tRISE | Rise time for any signal into test circuit(1)| 5ns | |
|---|---|---|---|
| tFALL | Rise time for any signal into test circuit(1)| 5ns | |

(1) tRISE and tFALL refer to a voltage change 10-90% of the peak to peak amplitude into a resistive load of 1k ohm and a capacitive load of 50 pF.

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Section 4.6, page 22

In this loading table, DIOR- and DIOW- are described as three-state signals. There should be some reference such that the host is responsible that these signals are always driven or pulled to a legal voltage. Floating signals on these critical inputs may produce unpredictable results.

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Section 5.1, page 24

In Table 5, the ground entry is not capitalized. As an absolute nit, it might look better if SPSYNC: and CSEL were on the same line.

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Section 5.2.4, page 25

The ATA specification started out as a description of the drive. It has turned into the description of the interface. In this context, the DMACK- signal is described as optional. For the signal input (the drive), the signal can be optional with no ill-effects. For the signal output (the host), if the signal is floating, an optional critical input may be floating, again producing unpredictable results. For the output, this totem-pole signal should be specified as driven or pulled high.

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Section 5.2.10, page 26

This section refers to the INTRQ signal and the conventions for negating it. The following text seems to be removed. Once upon a time, the drives were supposed to keep INTRQ asserted on an error or the last sector of a read operation. Is the consensus of the Working Group to remove this note?

Old text:
NOTE 3 Some drives may negate INTRQ on a PIO data transfer completion, except on a single sector read or on the last sector of a multi-sector read.

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Section 5.2.11, page 26

Wasn’t there a consensus that IOCS16- was not to be used by the host in PIO Mode 3 and higher speed PIO Modes?

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Section 5.2.12, page 26

In this paragraph, IORDY is described as floating when it is not being negated. In the loading table in Section 4.6, it is described as a three-state output. This paragraph needs to be extended.

Was:
When IORDY is not negated, IORDY shall be in a high impedance state.

Suggested:
When the drive is not in a valid register access or if neither DIOR- or DIOW- is asserted, IORDY shall be in a high impedance state.

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Section 6.3, page 30, and Section 6.3.7, page 32

These sections refer to the DRIVE ADDRESS register. I thought the Working Group consensus was to remove this register, leaving a note about previous implementations having used this address.

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Section 8, various pages

Another editorial comment, the term Vendor Specific is used in several places in this chapter, while the term Vendor Unique is defined in the Glossary. Should the term Vendor Unique be used, or should Vendor Specific be added to the Glossary, or should we leave well enough alone?

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Section 8.10.9, and Section 8.10.10, page 47

These paragraphs call out the register ordering from low to high, i.e. 23-24-25-26-28, and then suggest that the data in this field should be left justified. In this context, left, does not mean the same thing to all people. I suggest the following text. (BTW, the an was a minor mistake in the original)

Was:
The contents of this field are left justified an padded with spaces (20h).

Suggested:
The contents of this field are justified to the low address locations, and any unused locations are padded with spaces (20h).

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PIO Mode 4

This mode was not included in this revision. Was the intention to get Plenary permission first, or should the intention be to produce the document as the Working Group wishes it and after describing the significant changes, ask for forwarding?