94-076R0

TO: John Lohmeyer, Chairman, X3T10 Committee (SCSI)

From: Dennis Pak (408)974-4874
IEEE P1285 Liaison to X3T10/DADI

Date: March 18, 1994

Subject: P1285 Liaison Report for March 1994

## Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- Control and data space is memory mapped using P1212
- One controller, multiple slaves model
- Byte addressable, true memory mapped disk architecture
- Inherent spindle synchronization support
- Isochronous support
- Live insertion/removal
- Motherboard direct attach
- Scalability in performance and cost

## IEEE P1285 Project Status

The current activity involves defining the functional division between the memory unit (device) and the host/controller. Special emphasis has been given to PCI as a the physical portion of the beta level interface.

A member of Intel's PCI Architecture Group gave a briefing on PCI to the working group. Topics included:

378

- PCI as a System Bus
- PCI Interrupts
- Real-Time Attributes
- Limits of PCI
- Variations of PCI
- Who's Using PCI
- Heterogeneous PCI Architectures

The working group is also now examining a gamma level proposal for an SCI-like system as a means of working through issues related to DMA and the beta level. It is also about to consider a PC-like DMA structure as well.

A strawman proposal for a writeup of much of the discussion over the last several meetings associated with power control and error control was reviewed. A PCI document regarding the initialization and operation of a 1285/PCI interface was also reviewed.

An example multi-bridge system was discussed and the steps needed to initialize it were detailed. PCI-PCI bridges are being viewed as a means of extending the capability of a PCI bus to support more devices.

## Co-Located Meeting

In 1993 the co-located meetings with X3T10 occurred in May and November. Consequently, May 1994 might be the right choice for the next co-located meeting. Martin will coordinate this with John Lohmeyer.

## Upcoming Events

Future meetings are scheduled as follows:

April 7  Quantum Corp, 500 McCarthy Blvd, Milpitas, CA
May 5  Apple Computer, 1 Infinity Way, Cupertino, CA
June 2  Quantum Corp, 500 McCarthy Blvd, Milpitas, CA

These meetings are scheduled from 2:00-5:00 PM.