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_Subject: DMA Command Description Cleanup = 94-063r5

DMA Command Description Cleanup

Document 94-063r5

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All of the items discussed in this document are included in John Masiewicz's document 94-051r1. This will be the last revision of this document. This document is superceded by document 94-051r1.

This document was prepared for the 14 March 94 ATA Extension WG meeting in Newport Beach, CA.

--- The Round #5 Updated Issues List ---

Here is the final/last round of the DMA Definition discussion. Please recall that round #4 was discussed at the X3T9.2 meetings in Colorado Springs in November 1993.

For rounds #1 - #4 I used the ATA-1 Rev 4 section numbers. For round #5 I have switched to the ATA-2 (X3T9.2 948D rev 2) section numbers.

Here is my update list of issues by ATA-2 section number:

- * 5.2.9 DMARQ -- [See John Masiewicz's document 94-051r1.]
- * 8 Command descriptions -- The following paragraphs should be moved to section 9:
 - "If a new command is issued ... could have been completed."
 - "There shall be no indication ... New Command was issued."
- * 8.10.15 Word 52 -- [See John Masiewicz's document 94-051r1 and the SFF-8011 document.]
- * 8.16 Read DMA -- I recommend that the second paragraph of this section be replaced with the following text:

| During the execution of a Read DMA command, the drive shall
| provide status of BSY or DRQ until the command is completed.
|
| At command completion, the Command Block Registers contain the
| sector address of the last sector transferred.
|
| An unrecoverable error encountered during the execution of a
| Read DMA command results in the termination of the command.
| At command completion, the Command Block Registers contain the
| sector address of the sector where the first error occurred.

* 8.23 Set Features -- [SFF-8011 has addressed this issue.]

* 8.29 Write DMA -- I recommend that the second paragraph of this section be replaced with the following text:

| During the execution of a Write DMA command, the drive shall
| provide status of BSY or DRQ until the command is completed.

| At command completion, the Command Block Registers contain the
| sector address of the last sector transferred.

| An unrecoverable error encountered during the execution of a
| Write DMA command results in the termination of the command.
| At command completion, the Command Block Registers contain the
| sector address of the sector where the first error occurred.

* 9 Protocol --

This section describes what happens when one command is interrupted by another command.

The following paragraphs should be moved here from section 8:

| If a new command is issued ... could have been completed.

| There shall be no indication ... New Command was issued.

It is not possible to interrupt a Read DMA or Write DMA command with another command. The only way to interrupt a DMA command is with a reset. I recommend the following be added to this section:

| The only way to interrupt a Read DMA or Write DMA command is
| with a reset. The result of interrupting a Read DMA or Write
| DMA command by writing a new command into the Command register
| is unpredictable.

* 9.5 DMA Data Transfer Command -- I recommend the that the text of this section be replaced by the following text:

| 10.5 DMA data transfer commands (optional)

| This class comprises:

- | - Read DMA
- | - Write DMA

| Data transfers using DMA commands differ in two ways from PIO transfers:

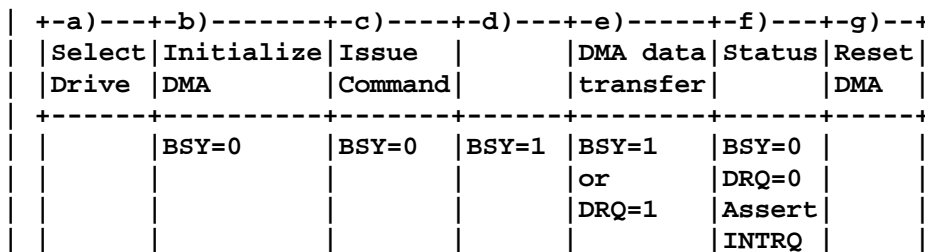
- | - data transfers are performed using the slave-DMA channel
- | - a single interrupt is issued at the completion of the command

| Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

| The interrupt handler for DMA transfer is different in that no intermediate sector interrupts are issued on multi-sector commands.

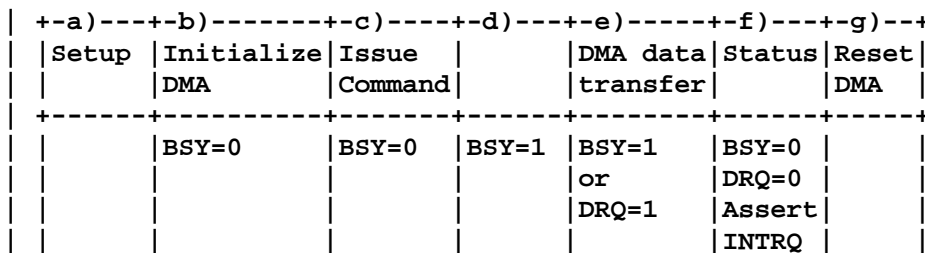
- a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
- b) The host initializes the slave-DMA channel.
- c) The host writes the command code to the Command register.
- d) The drive sets BSY.
- e) When the drive is ready to transfer data, the drive asserts DMARQ. The DMA data transfer may be split into several partial transfers at the discretion of the drive or slave-DMA channel. The drive shall assert either BSY or DRQ during the entire DMA data transfer phase.
- f) When the drive has completed processing, it clears both BSY and DRQ and asserts INTRQ. The host reads the Status register.
- g) The host resets the slave-DMA channel.

* 9.5.1 Normal DMA Transfer -- I recommend that the diagram be replaced with the following diagram:



* 9.5.2 Aborted DMA transfer -- I recommend that this section be replaced by:

9.5.2 DMA transfer terminated by an error during data transfer.



* 9.5.3 Aborted DMA command -- I recommend that this section be replaced by:

9.5.3 DMA command terminated by an error before any data is transferred.

