

Date: Fri Feb 25 11:20:22 199 PST X3T10/94-058r0
From: John Masiewicz <John_Masiewicz@notes.seagate.com>
To: ata@dt.wdc.com
Subject: Word 51,52, 64, 66 Revisions for comments.
Extracted-To: ATA_Reflector

The following are comments are on X3T9.2, document 0948D Revision 2 dated Jan 1, 1994.

I believe all of the comments are editorial, and do not present new information, but clarify agreed-upon intent. Comments are welcome.

Page 50 Section 8.10.14 STATES:

8.10.14 Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 6 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 6, and if it does not, then Mode 0 shall be used to serve as the default timing.

COMMENT: The figure referred to (figure 6) is incorrect. It should refer to figure 5 (PIO data transfer). Also, figure 5 now includes mode 3. The agreement for word 51 was that it would only be used for the original PIO modes, i.e. modes 0,1, and 2. Higher modes would not be allowed in word 51 for ATA-1 compatibility. This is referred to in a note in word 64 (page 51). The note should also be clarified to refer to PIO modes 0-2 instead of "original PIO modes". I believe this is an editorial issue and I am not recommending anything new other than clarification.

RECOMMENDATION: Correct paragraph 8.10.14 and add corrected note below:

8.10.14 Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 5 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 2 categories specified in figure 5, and if it does not, then Mode 0 shall be used to serve as the default timing.

Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

Page 50 Section 8.10.15 States:

8.10.15 Word 52: DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 6 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 6, and if it does not, then Mode 0 shall be used to serve as the default timing.

The contents of this word shall be ignored if Words 62 or 63 are supported.

COMMENT: Figure 6 is Single Word DMA, and the Description is not very specific that this word refers only to SINGLE-WORD DMA transfer timing mode.

RECOMMENDATION: Clarify wording to state Single word DMA, and add clarification parenthesis to paragraph as shown below as shown below:

8.10.15 Word 52: Single Word DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 6 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 6 (i.e. 0,1, or 2), and if it does not, then Mode 0 shall be used to serve as the default timing.

The contents of this word shall be ignored if Words 62 or 63 are supported.

Page 51 Section 8.10.25 STATES:

8.10.25 Word 64: Flow Control PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Drive parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes that it is capable of supporting.

Of these bits, bits 7 through 1 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3.

Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode it can support.

COMMENT: Reference in Note to "highest original PIO mode" is unclear.

RECOMMENDATION: Revise note to say:

Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

Page 52 Section 8.10.27 STATES:

8.10.27 Word 66: Manufacturer's Recommended Multiword DMA Cycle Time

Word 66 of the parameter information of the IDENTIFY DRIVE command is defined as the Manufacturer's Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under nominal conditions.

If a host attempts to run at a faster cycle rate by operating at a cycle time of less than this value, the device may be forced to negate DMARQ to prevent data corruption. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate.

If this field is supported, bit 1 of word 53 must be set.

Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

COMMENT:

The second paragraph is confusing. Marketing types object to any reference of data corruption and say it suggests that anything faster than Word 66 cycle time WILL result in corruption. Some other people say that Word 66 is the rate at which DMARQ will NEVER be deasserted. They compare it to running PIO without IORDY support. Neither of these arguments is correct, but the paragraph could be interpreted in many ways.

RECOMMENDATION: Rewrite paragraph to say:

If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance MAY result.

--

John Masiewicz (John_Masiewicz@notes.seagate.com)

Seagate Technology - 920 Disc Drive - Scotts Valley, CA 95066 USA
Main Phone 408-438-6550 - Email Problems postmaster@notes.seagate.com
Technical Support: BBS 408-438-8771 Fax 408-438-8137 Voice 408-438-8222
