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_Subject: X3T10/94-051r1 (ATA-2 Draft Comments revision 1)

This document contains the recommended changes from my original documents:

X3T10/94-051r0 dated 2/18/94 (Subject: Comments / Recommendations on ATA-2 Working Draft)

X3T10/94-058r0 dated 2/25/94.(Subject Word 51,52,64,66 Revisions for Comments)

This revision also contains previously agreed-upon changes from Hale Landis' document:

X3T9/92-110r5 dated 3/10/94 (Subject: DMA Command Description Cleanup)

I have included each affected paragraph or section with the changes edited in.

At the next meeting I will distribute a hard copy which highlights the differences with strike-outs & additions.

All comments are against the X3T9.2/0948D revision 2 document.

4.2.2 3-pin power

The pin assignments are shown in table 2. Recommended part numbers for the mating connector to 18 AWG cable are shown below, but equivalent parts may be used.

Connector (3 pin) Molex 5484 39-27-0032 or equivalent.

[Editor's Note: Is this the device side connectors or the cable side connectors?]

Power Line Designation	Pin Number
+5 Volts	1
+12 Volts	2
Ground	3

Table 2 - DC Interface Using 3 Pin Power Connector

[Editor's Note: How do we specify the pin one orientation?]

4.6 DC Characteristics

	Description	Min	Max
IoL	Driver sink current for 5V operation	12mA	
IoH	Driver source current	-400uA	
Vih	Voltage Input High	2,0 V	
Vil	Voltage Input Low		0,8 V
Voh	Voltage Output High (Ioh = -400 u A)	2,4 V	
Vol	Voltage Output Low (5V, Iol = 12ma)		0,5 V
Cin	Input Capacitance (of Device)		25 pf
Cout	Output Capacitance (of Device)		25 pf

Table 3A - DC Characteristics

	Description	Min	Max
tRISE	Rise time for any signal on AT interface(1)	5ns	
tFALL	Rise time for any signal on AT interface(1)	5ns	

(1) tRISE and tFALL are measured from 10-90% of full signal alplitude with a total capacitive load of 100 pF.

Table 3B - AC Characteristics

[Editor's note: IoH value at 400 uA is insufficient at least in the case of DMARQ which is typically pulled low by a 5.6k resistor.]

X.X.X ATA-2 Driver Types and Required Pull-ups

Signal	Source	Driver Type (1)	Pull-up at Host (2)	Pull-up at each Device(2)	Notes
Reset	Host	TP			
DD 0:15	Bidir.	TS			
DMARQ	Device	TS	5.6K PD		(3)
DIOR- DIOW-	Host	TS			
IORDY	Device	TS	1.0K		(4)
SPSYNC/CSEL					(5)
CSEL	Host		Ground	10K	(6)
SPSYNC	Device	TS/OC		VU	(7)
DMACK-	Host	TP			
INTRQ	Device	TS			
IOCS16-	Device	OC	1.0K		
DA0:2	Host	TP			
PDIAG-	Device	TS		10K	
CS0- CS1-	Host	TP			
DASP-	Device	OC		10K	(5)

+=====+=====+=====+=====+=====+=====+

- (1) TS=Tri-State; OC=Open Collector; TP=Totem-Pole; PU=Pull-up; PD=Pull-down; VU=Vendor Unique
- (2) All resistor values are minimum (lowest) allowed.
- (3) ATA-2 defines this line to be tri-stated whenever the device is not selected or is not executing a DMA data transfer. When enabled by DMA transfer, it will be driven high and low by the device.
- (4) This signal should only be enabled during DIOR/DIOW cycles to the selected device.
- (5) See signal descriptions for information on dual use of this signal.
- (6) When used as CSEL, Line is grounded at Host and 10K Pull-up is required at both devices.
- (7) When Used as SPSYNC, application is vendor unique.

Table x - ATA-2 Driver Types and Required Pull-ups

5.2.8 DMACK- (DMA acknowledge) (Optional)

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

NOTE: This signal may be deasserted by the Host to suspend the DMA transfer in process. For Multi-Word DMA transfers, the Device may deassert DMARQ within the tL specified time (refer to Figure 7 pg. 71) once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the Device may leave DMARQ asserted and wait for the Host to reassert DMACK-.

5.2.9 DMARQ (DMA request) (Optional)

This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e. the drive shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line will be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it will be driven high and low by the device.

When a DMA operation is enabled, IOCS16-, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

NOTE: In ATA-1 devices, this signal was either totem-pole or tri-state in different implementations. In EISA systems, 5.6K pull-down is used to cause a logic low on undriven lines. ATA-2 defines this line to be in high-impedance mode except when DMA transfer is active from the selected drive.

In systems which may use mixed devices where totem-pole drivers are used, and the system shares this line with other non-ATA devices, the ATA host or ATA adapter shall ensure that appropriate protection is employed to protect ATA device DMARQ drivers from damage.

5.2.10 INTRQ (Drive interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control register. If nIEN=1, or the drive is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

INTRQ shall be negated by:

- assertion of RESET- or
- the setting of SRST of the Device Control register, or
- the host writing the Command register or
- the host reading the Status register

On PIO transfers, INTRQ is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the SET MULTIPLE MODE command. An exception occurs on FORMAT TRACK, WRITE SECTOR(S), WRITE BUFFER and WRITE LONG commands - INTRQ shall not be asserted at the beginning of the first data block to be transferred.

On DMA transfers, INTRQ is asserted only once, after the command has completed.

If the system shares this line with non-ATA devices, the ATA host or ATA adapter shall ensure that appropriate protection is employed to protect ATA device INTRQ drivers from damage.

5.2.12 IORDY (I/O channel ready) (Optional)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the drive is not ready to respond to a data transfer request.

If actively asserted, this signal shall only be enabled during DIOR-/DIOW-cycles to the selected drive. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

8. Command Descriptions

Commands are issued to the drive by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command register.

The manner in which a command is accepted varies. There are three classes (see table 9) of command acceptance, all predicated on the fact that to receive a command, BSY=0:

Upon receipt of a Class 1 command, the drive sets BSY within 400 nsec. Upon receipt of a Class 2 command, the drive sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 usec, and

clears BSY within 400 nsec of setting DRQ.

Upon receipt of a Class 3 command, the drive sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec, and clears BSY within 400 nsec of setting DRQ.

NOTE: DRQ may be set so quickly on Class 2 and Class 3 that the BSY transition is too short for BSY=1 to be recognized.

The drive shall implement all mandatory commands as identified by an M, and may implement the optional commands identified by an O, in table 9. V indicates a Vendor Specific command code.

		-----Command-----Parameters						
Used=====+								
Class		code	FR	SC	SN	CY	DH	
1	ACKNOWLEDGE MEDIA CHANGE	O DBh					D	
1	BOOT - POST-BOOT	O DCh					D	
1	BOOT - PRE-BOOT	O DDh					D	
1	CHECK POWER MODE	O 98h E5h		y			D	
1	DOOR LOCK	O DEh					D	
1	DOOR UNLOCK	O DFh					D	
3	DOWNLOAD MICROCODE	O 92h	y	y	y	y	D	
1	EXECUTE DRIVE DIAGNOSTIC	M 90h						
D*	2	M 50h	*	y		y	y	
1	IDENTIFY DRIVE	O ECh					D	

| CY = Cylinder registers SC = Sector Count register

| DH = Drive/Head register SN = Sector Number register

| FR = Features register (see command descriptions for use)

| y - the register contains a valid parameter for this command.

| For the Drive/Head register, y means both the drive and

| head parameters are used.

| D - only the drive parameter is valid and not the head parameter.

| D* - Addressed to drive 0 but both drives execute it.

| * - Maintained for compatibility (see 7.2.10)

|
+-----
=+

Table 9 - Command Codes and Parameters

(Part 1 of 2)

8.10.14 Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 5 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 2 categories specified in figure 5, and if it does not, then Mode 0 shall be used to serve as the default timing.

Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

Word 52: Single Word DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in figure 6 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in figure 6 (i.e. 0, 1, or 2), and if it does not, then Mode 0 shall be used to serve as the default timing.

The contents of this word shall be ignored if Words 62 or 63 are supported.

8.10.25 Word 64: Flow Control PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Drive parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes that it is capable of supporting.

Of these bits, bits 7 through 1 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3.

Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

8.10.27 Word 66: Manufacturer's Recommended Multiword DMA Cycle Time

Word 66 of the parameter information of the IDENTIFY DRIVE command is defined as the Manufacturer's Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under nominal conditions.

If a host runs at a faster cycle rate by operating at a cycle time of less than

this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance MAY result.

If this field is supported, bit 1 of word 53 must be set.

Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.16. READ DMA

This command executes in a similar manner to the READ SECTOR(S) command except for the following:

- the host initializes a slave-DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- the drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a Read DMA command, the drive shall provide status of BSY or DRQ until the command is completed.

At command completion, the Command Block Registers contain the sector address of the last sector transferred.

An unrecoverable error encountered during execution of a READ DMA command results in the termination of the command. At command completion, the Command Block Registers contain the sector address of the sector where the first error occurred.

8.29 WRITE DMA

This command executes in a similar manner to WRITE SECTOR(S) except for the following:

- the host initializes a slave-DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- the drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write DMA command, the drive shall provide status of BSY or DRQ until the command is completed.

At command completion, the Command Block Registers contain the sector address of the last sector transferred.

An unrecoverable error encountered during the execution of a Write DMA

command

results in the termination of the command. At command completion, the Command Block Registers contain the sector address of the sector address of the sector where the first error occurred.

9. Protocol

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if BSY=1, and should proceed no further unless and until BSY=0. For most commands, the host will also wait for DRDY=1 before proceeding. Those commands shown with DRDY=x can be executed when DRDY=0.

Data transfers may be accomplished in more ways than are described below, but these sequences should work with all known implementations of ATA drives.

If a new command is issued to a drive which has an uncompleted command (subsequently referred to as Old Command) in progress, the drive shall immediately respond to the new command (Subsequently referred to as New Command), even if execution of the Old Command could have been completed.

There shall be no indication given to the system as to the status of the Old Command which was being executed at the time the New Command was issued.

The only way to interrupt a Read DMA or Write DMA command is with a reset. The result of interrupting a Read DMA or Write DMA command by writing a new command into the Command Register is unpredictable.

9.5 DMA data transfer commands (optional)

This class comprises:

READ DMA
WRITE DMA

Data transfers using DMA commands differ in two ways from PIO transfers:
data transfers are performed using the slave-DMA channel
A Single interrupt is issued at the completion of the command.

Initiation of the DMA transfer commands is identical to the READ SECTOR(S) or WRITE SECTOR(S) commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that no intermediate sector interrupts are issued on multi-sector commands

- a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
- b) The Host initializes the slave-DMA channel
- c) The host writes the command code to the Command register.

d) The drive sets BSY.

e) When the drive is ready to transfer data, the drive asserts DMARQ. The DMA data transfer may be split into several partial transfers at the discretion of

the drive or slave-DMA channel. The drive shall assert either BSY or DRQ during the entire DMA data transfer phase.

f) When the drive has completed processing, it clears both BSY and DRQ and asserts INTRQ. The host reads the Status Register.g) Host resets the slave-DMA channel

9.5.1 Normal DMA transfer

+a)---+b)-----+c)-----+d)---+e)-----+f)---+g)---+
Setup Initialize Issue DMA data Status Reset
DMA Command transfer DMA
+-----+-----+-----+-----+-----+-----+-----+
BSY=0 BSY=0 BSY=1 BSY=1 BSY=0
or DRQ=0
DRQ=1 Assert
INTRQ

9.5.2 DMA Transfer terminated by an error during data transfer.

+a)---+b)-----+c)-----+d)---+e)-----+f)---+g)---+
Setup Initialize Issue DMA data Status Reset
DMA Command transfer DMA
+-----+-----+-----+-----+-----+-----+-----+
BSY=0 BSY=0 BSY=1 BSY=1 BSY=0
or DRQ=0
DRQ=1 Assert
INTRQ

9.5.3 DMA Command terminated by an error before any data is transferred.

+a)---+b)-----+c)-----+d)---+f)---+g)---+
Setup Initialize Issue Status Reset
DMA Command DMA
+-----+-----+-----+-----+-----+-----+
BSY=0 BSY=0 BSY=1 BSY=0
DRQ=0
Assert
INTRQ

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