Date: March 31, 1994
From: Tom Hanan, Western Digital
Updated by: Steve Finch for presentation to X3T10 Plenary
TO: X3T10 ATA Working Group and SFF ATAPI Project Group
Subject: Updated Mode 4 16.6 MB/s timing for ATA-2

Per our original agreement, I am continuing to distribute this timing information to both memberships. The intent is to solicit as many inputs from as many industry groups as possible.

This information was updated at the ATA Working Group meeting on Monday, March 14. The ATA Working Group feels this information is technically complete, and should be included in the proposed ATA-2 standard.

The timing information contained in this document has been stable for approximately two months, and has been agreed to by the ATA Working Group. Minor changes have been made to the text and timing charts for clarification.

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The minimum cycle time supported by the device in PIO Mode 3, 4 and Multiword DMA Mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated Mode e.g. a drive supporting PIO Mode 4 timing shall not report a value less than 120 nanoseconds, the minimum cycle time defined for Mode 4 PIO Timings.

x.1 New Multiword DMA Transfer Mode

The new Multiword DMA Transfer Mode is Mode 2.

x.1.1 Timing Parameters

The timing parameters associated with Multiword DMA Transfer Mode 2 are defined in Table x-1. Peripherals reporting support for Multiword DMA Transfer Mode 2 shall also support Multiword DMA Transfer Mode 0 and 1.

TABLE x-1 MULTIWORD DMA TIMING PARAMETERS

	Multiword DMA timing parameters		Mode 2 nsec	
			Min	Max
t0	Cycle time	*3	120	
tC	DMACK to DMREQ delay			---
tD	DIOR-/DIOW- 16-bit	*3	70	
tE	DIOR- data access			---
tF	DIOR- data hold		5	
tF	DIOR- data hold	*1		n/a
tGr	DIOR- data setup		20	
tGw	DIOW- data setup		20	
tH	DIOW- data hold		10	
tI	DMACK to DIOR-/DIOW- setup		0	
tJ	DIOR-/DIOW- to DMACK hold		5	
tK	DIOR-/DIOW- negated width	*3	25	
tLr	DIOR- to DMREQ delay			35
tLw	DIOW- to DMREQ delay			35
tZ	DMACK- to tristate	*2		25

*1 The meaning of this parameter in ATA was not clear. The parameter is not applicable to this Specification.

*2 This parameter specifies the time from the negation edge of DMACK- to the time the data bus is no longer driven by the device (tristate). The tZ parameter applies only at the end of a Multiword DMA cycle, i.e. when DMACK is negated. The device may actively drive the data bus or may tristate the data bus while DMACK- is active from the first time that DIOR- is asserted until DMACK- is deasserted as long as tE and tF requirements are met.

*3 t0 is the minimum total cycle time, tD is the minimum command active time, and tK is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tK shall be met. The minimum total cycle time requirement, t0, is greater than the sum of tD and tK. This means a host implementation can lengthen either or both tD or tK to ensure that t0 is equal to the value reported in the devices identify drive data.~~met~~. A device implementation shall support any legal host implementation.

x.1.2 Timings

The timings associated with Multiword DMA Transfers are defined in Figure x-1, and include the new timing parameter tZ. The minimum value of t0 is specified by word 65 in the Identify Drive parameter list. Note that the edge used to measure T0 was changed from asserted to de-asserted in order to make the timing diagrams more closely reflect real VLSI and system timing issues.

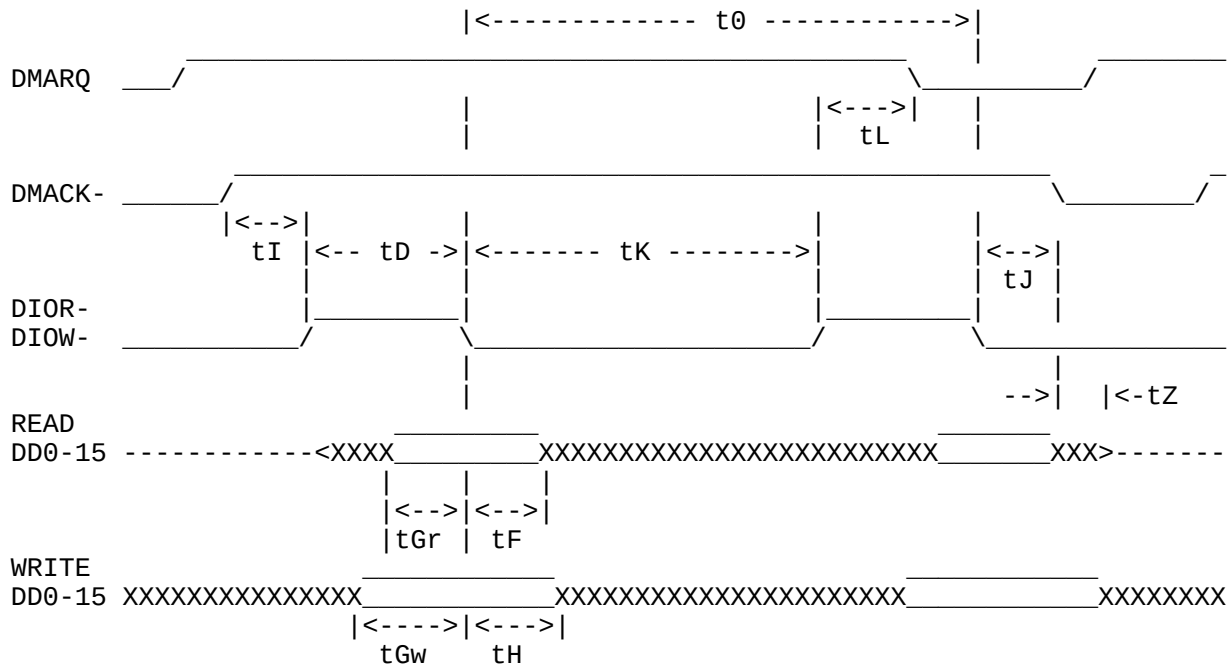

FIGURE x-1 MULTIWORD DMA TIMING DIAGRAM

x.2 New PIO Transfer Mode

The new PIO Transfer Mode is Mode 4.

x.2.1 Timing Parameters

The timing parameters associated with PIO Transfer Mode 4 are defined in Table x-2. Peripherals reporting support for PIO Transfer Mode 4 shall power up in a PIO Transfer Mode compatible with ATA.

TABLE x-2 PIO TIMING PARAMETERS

	PIO timing parameters		Mode 4 nsec Min	Mode 4 nsec Max
t0	Cycle time	*4	120	
t1	Address valid to DIOR-/DIOW- setup		25	
t2	DIOR-/DIOW- 16-bit	*4	70	
	Pulse width 8-bit	*4	70	
t2i	DIOR-/DIOW- recovery time	*4	25	
t3	DIOW- data setup		20	
t4	DIOW- data hold		10	
t5	DIOR- data setup		20	
t6	DIOR- data hold		5	
t6	DIOR- data hold	*1		n/a
t6Z	DIOR- data tristate	*2		30
t7	Addr valid to IOCS16- assertion			30
t8	Addr invalid to IOCS16- Release			25
t9	DIOR-/DIOW- to address valid hold		5	
tA	IORDY Setup time	*3	25	
tB	IORDY Pulse Width			1,250
tRD	Read Data Valid to IORDY active (if IORDY initially low after tA)		0	

*1 The meaning of this parameter in ATA was not clear. The parameter is not applicable to this Specification.

*2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tristate).

*3 The delay from DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.

*4 t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, t2i shall be met. The minimum total cycle time requirement, t0, is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

x.2.2 Timings

The timings associated with PIO Mode 4 transfers are defined in Figure x-2, and include the new timing parameters t2i, t6Z and tR. The minimum value of t0 is specified by word 68 in the Identify Drive parameter list (see 7.1.8). Note that the edge used to measure T0 was changed from asserted to de-asserted in order to make the timing diagrams more closely reflect real VLSI and system timing issues.

It is mandatory that IORDY be supported when PIO Mode 3 or 4 are the current mode of operation.

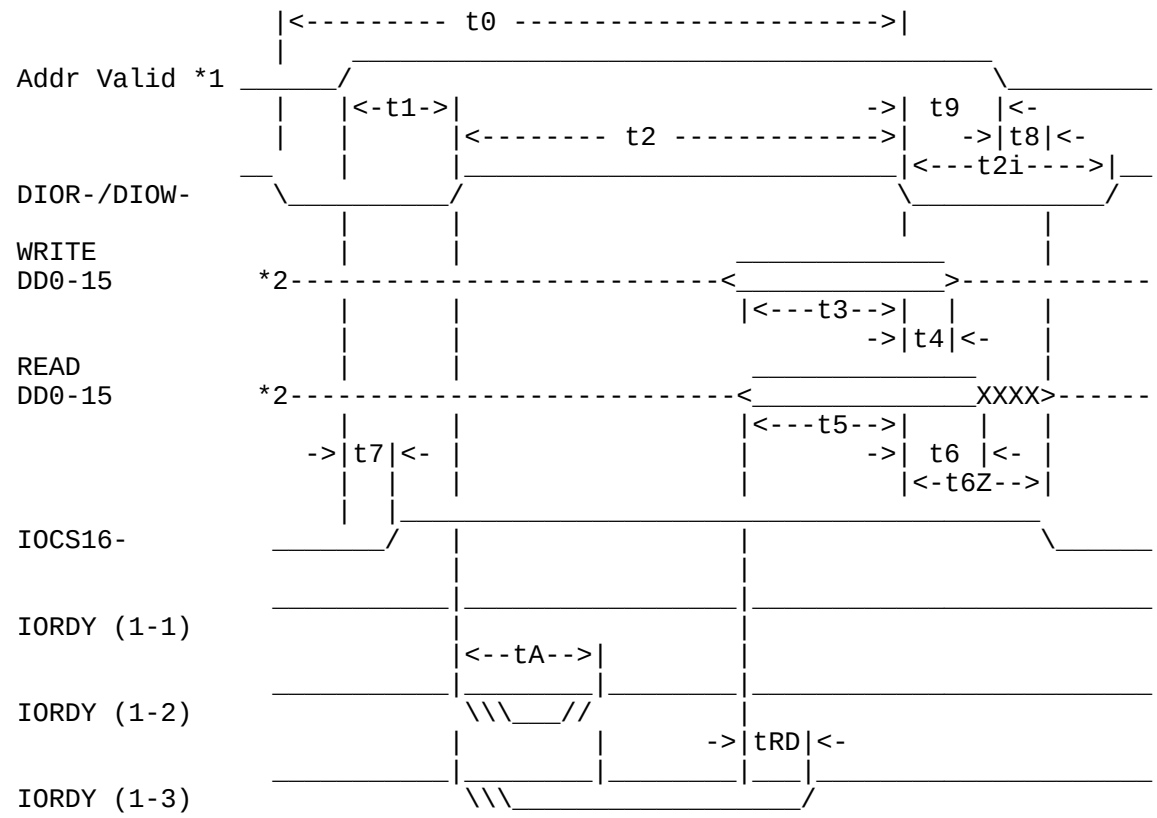

FIGURE x-2 PIO TIMING DIAGRAM

Notes:

(1) The deassertion of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-. The assertion and deassertion of IORDY are described in the following three cases:

(1-1) Device never deasserts IORDY: no wait is generated.

(1-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: no wait generated.

(1-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, device must place read data on DD0-15 for tRD before causing IORDY to be asserted.

y. Command and Parameter Changes

Changes to the Identify Drive Command

y.1 Word 64: Flow Control PIO Transfer Modes Supported

Word 64 Bits 7-0 is a bit significant field. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes it is capable of supporting. Bits 7-2 are reserved for future use.

- If Bit 0=1, the device supports PIO Mode 3.
- If Bit 1=1, the device supports PIO Mode 4.

NOTE: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode it can support.

y.2 Word 65: Minimum Multiword DMA Transfer Cycle Time Per Word

Word 65 defines the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

If this field is supported, Word 53 Bit 1=1 shall be set.

Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time reported by the fastest DMA mode supported by the device.

If Word 53 Bit 1=1 because a drive supports a field in Words 64-70 other than this field, the device shall return a value of zero in this field.

y.3 Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

Word 67 defines the minimum cycle time that the device guarantees shall not cause data integrity degradation during a transfer which does not utilize flow control.

Any device may support this field, and if this field is supported, bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in Word 67 shall not be less than the value reported in word 68.

If Word 53 Bit 1=1 because a drive supports a field in Words 64-70 other than this field, the device shall return a value of zero in this field.

y.4 Word 68: Minimum PIO Transfer Cycle Time With IORDY Flow Control

Word 68 defines the minimum cycle time that the device can support when performing data transfers while utilizing IORDY flow control.

Any device may support this field, and if this field is supported, bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 68 shall not be less than the fastest PIO mode reported by the device.

If Word 53 Bit 1=1 because a drive supports a field in Words 64-70 other than this field, the device shall return a value of zero in this field.