

TO: John Lohmeyer, Chairman, X3T10 Committee (SCSI)
From: Dennis Pak (408)974-4874
IEEE P1285 Liaison to X3T10/DADI
Date: January 14, 1994
Subject: **P1285 Liaison Report for January 1994**

X3T10/94-037r0

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o One controller, multiple slaves model
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

The current activity involves specifying the mapping to two physical levels: PCI and RamLink. Work continues on the P1285 command structure and adding some new commands. The P1285 document continues to be refined.

In November the P1285 document was posted on ftp site [hplsci.hpl.hp.com](ftp://hplsci.hpl.hp.com/pub/P1285/latest_ps) in directory [pub/P1285/latest_ps](ftp://hplsci.hpl.hp.com/pub/P1285/latest_ps). An update to that posting is slated for sometime in February.

A co-located meeting between X3T9.2 and P1285 was held in November and a number of suggestions were made that are currently being acted on. These include support for error logging and support for testing the result of an exclusive-OR operation. The latter is helpful in array applications.

Several specific topics have been discussed recently. These topics include power management, interrupt structure, exclusive access of devices and error handling.

The issue of the P1285 acronym was also discussed.

Upcoming Events

P1285 tentative meeting dates and locations:

February	3 HP Labs, Peter Coutts Rd, Bldg 3, Palo Alto, CA
March	3 Apple Computer, 1 Infinite Loop, Cupertino, CA
April	7 Quantum Corp, 500 McCarthy Blvd, Milpitas, CA

These meetings are scheduled from 2:00-5:00 PM.