TO: **ATA-3 Working Group** **X3T10/94-027r3**
SUBJECT: **Error Detection Using Data CRC**
FROM: **R. Kalish   408-957-7169**
DATE: **November 20, 1994**

The enhanced transfer modes in ATA-2 and those proposed for ATA-3 need a reliable method to detect errors in the data transferred across the cable to verify that it was received correctly and was not corrupted.

This proposal suggests adding four new commands for READ/WRITE-MULTIPLE W/CRC and READ/WRITE DMA W/CRC. Since the current READ/WRITE-MULTIPLE and READ/WRITE DMA commands are optional, these new commands would also be optional.

1. READ Multiple W/CRC - Command Code CCh

The new command for Read Multiple W/CRC will transfer 516 bytes of data per sector from the drive to the host.

2. WRITE Multiple W/CRC - Command Code CDh

The new command for Write Multiple W/CRC will transfer 516 bytes of data per sector from the host to the drive. A bad transfer will result in an error flag in both status registers for the status of the operation.

3. READ Multiple DMA W/CRC - Command Code CEh

The new command for Read Multiple DMA W/CRC will transfer 516 bytes of data per sector from the drive to the host. This command will abort if the drive is not set up for Multiple Mode DMA.

4. WRITE Multiple DMA W/CRC - Command Code CFh

The new command for Write Multiple DMA W/CRC will transfer 516 bytes of data per sector from the host to the drive. A bad transfer will result in an error flag in both status registers for the status of the write operation. This command will abort if the drive is not set up for Multiple Mode DMA.

5. CRC Polynomial

The 4 byte CRC polynomial is the same as used for P1394 (and many other specifications) which should be universally acceptable (We will not discuss the merits of this number since there are only a very few people who fully understand the pros and cons of this polynomial versus another, and we are not in that group).

The CRC has the following properties:

Generator Polynomial:

$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
CRC Register is preset to all 1's before generation and checking.

Generated CRC Redundancy Polynomial:

R$(x) = one's complement of the remainder polynomial of degree less than 32, i.e. the remainder is inverted before being shifted out.

Check Polynomial produced by the receiver upon receiving an error-free sequence (data and CRC redundancy):

$C(x) = x^{31} + x^{30} + x^{26} + x^{25} + x^{24} + x^{18} + x^{15} + x^{14} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^4 + x^3 + x + 1$

6.   General Requirements

The drive must be previously set in the multiple mode or all of the above commands will abort. These commands will be used on a sector by sector block of data. The process of generating and checking the

CRC would most likely be implemented with logic in a bridge adapter appending the CRC on a disk write and check the CRC on a disk read. If there is a CRC error when reading data from the disk, the host bridge logic will be required to notify the host of the error. We can propose the exact method for this, or leave the implementation up to the bridge designer since this will require BIOS modification or Driver support anyway. Our earlier proposal of letting the host microprocessor generate and check the CRC would probably cause a major time and resource burden to the system.

7.   Drive Requirements

The drive will need two bits in the Identify Drive Parameter Information to specify that the drive can support the Read/Write Multiple W/CRC and the Read/Write Multiple DMA W/CRC commands. A likely place is in Word 49 bits 13 and 14 since this word is specifying drive capabilities, but there is no hard reason for not putting this information elsewhere. We are assuming that if a drive will support a Read W/CRC that it must support the Write W/CRC also, but the drive does not have to support both the PIO and DMA modes if it supports one.