X3T10/94-027

TO: X3T9.2 ATA Local Bus Working Group

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RE: Proposal for Data CRC across the Cable

ATA PIO Mode 4 an Multi-word DMA Mode 2 need a reliable method to verify the data transferred across the cable was received properly and was not corrupted. This feature has long been a part of the SCSI interface with the parity bit enabling the verification of each byte of data. Since there is no room on the cable for parity on each byte of a data transferred, Al and I would like to propose a method for data integrity verification across the cable. This would mean adding 4 new commands for Read/Write-Multiple (W/CRC) and Read/Write DMA (W/CRC) and only be for the high speed modes (20 Mbytes/sec transfer rates). Since the current Read/Write-Multiple and DMA commands are optional, these new commands would also be optional.

We are proposing the following:

1. READ Multiple W/CRC - Command Code CCh

   The new command for Read Multiple W/CRC will cause a transfer of 516 bytes of data from the drive to the host. The host system microprocessor is required to scan the data and verify the CRC to insure the transfer was not corrupted.

2. WRITE Multiple W/CRC - Command Code CDh

   The new command for Write Multiple W/CRC will cause a transfer of 516 bytes of data from the host to the drive. The host system microprocessor is required to generate a CRC appended to the 512 bytes of data and the drive must verify the CRC to insure the transfer was not corrupted. A bad transfer will result in an error flag in both status registers for the status of the operation.

3. READ Multiple DMA W/CRC - Command Code CEh

   The new command for Read Multiple DMA W/CRC will abort if the drive is not set up for Multiple Mode DMA and will transfer 516 bytes of data from the drive to the host. The host system microprocessor is required to scan the data and verify the CRC to insure the transfer was not corrupted.

4. WRITE Multiple DMA W/CRC - Command Code CFh

   The new command for Write Multiple DMA W/CRC will abort if the drive is not set up for Multiple Mode DMA and will cause a transfer of 516 bytes of data from the host to the drive. The host system microprocessor is required to generate a CRC appended to the 512 bytes of data and the drive must verify the CRC to insure the transfer was not corrupted. A bad transfer will result in an error flag in both status registers for the status of the write operation.

5. CRC Polynomial

The 4 byte CRC polynomial is the same as used for P1394 (and probably many other specifications) which should be universally acceptable. The CRC has the following properties:

- Generator Polynomial:
  G(x) = x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1

- CRC Register is preset to all 1's before generation and checking.

- Generated CRC Redundancy Polynomial:
  R$(x) = one's complement of the remainder polynomial of degree less than 32, i.e. the remainder is inverted before being shifted out.

- Check Polynomial produced by the receiver upon receiving an error-free sequence (data and CRC redundancy):
  C(x) = x^31 + x^30 + x^26 + x^25 + x^24 + x^18 + x^15 + x^14 + x^12 + x^11 + x^10 + x^8 + x^6 + x^5 + x^4 + x^3 + x + 1

6. General Requirements

The drive must be previously set in the multiple mode or all of the above commands will abort. These commands will be used on a sector by sector block of data and verified by the host microprocessor. This will eliminate the extra circuitry requirement of a host adapter to handle the CRC on the data. Since the burden for checking the data is upon the host, this will require a BIOS or driver which knows about the new commands and also a Identify Drive feature to let the host know that the drive can support the new transfer modes.

7. Drive Requirements

The drive will need two bits in the Identify Drive Parameter Information to specify that the drive can support the Read/Write Multiple W/CRC and the Read/Write Multiple DMA W/CRC commands. A likely place is in Word 49 bits 13 and 14 since this word is specifying drive capabilities, but there is no hard reason for not putting this information elsewhere. We are assuming that if a drive will support a Read W/CRC that it must support the Write W/CRC also, but the drive does not have to support both the PIO and DMA modes if it supports one.