An Idea for 6G Implementation

Dynamic signal line Length Compensation (DLC)

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Storage Product　FUJITSU

1/14/08

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Background

-SAS 6G Implementation is real tough work

Wave form is drastically changed by line length & frequency.

Line length can change by simply swapping a HDD slot position.

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We should change and adjust signal condition on case by case.

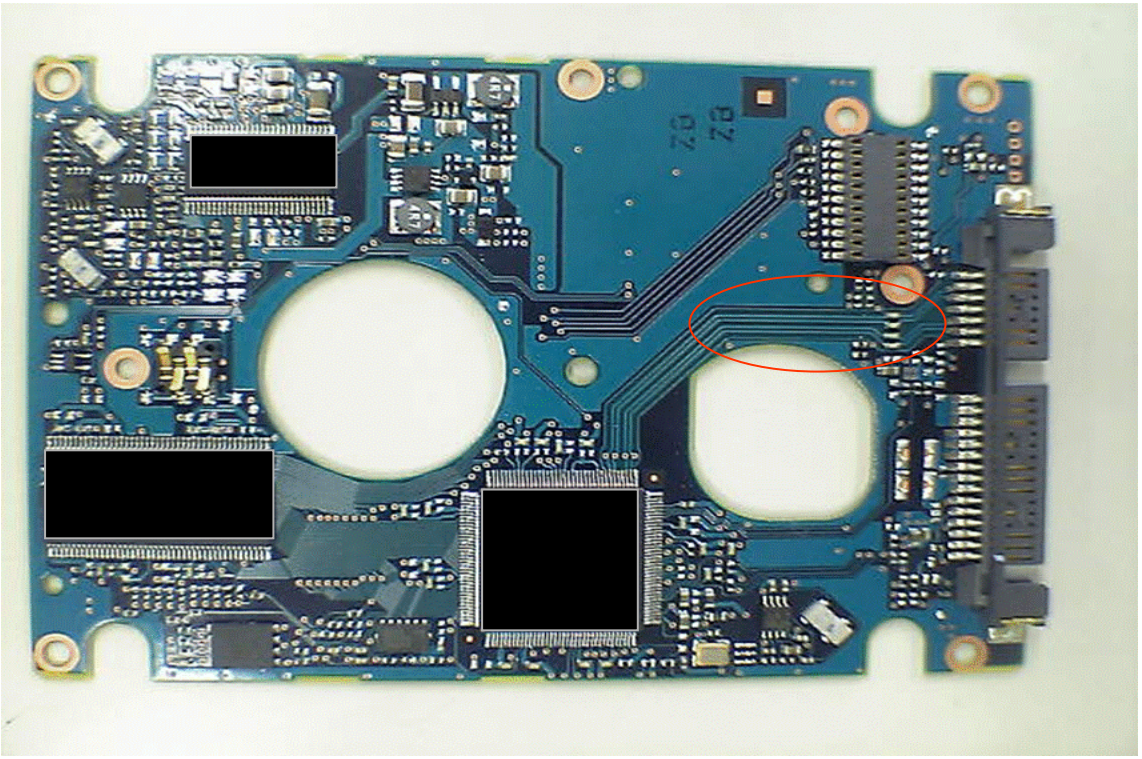
But it is difficult in real usage.

Background (continued)

-HDD have to support four line within <10 mm PCB space.

Cross talk between the link induced Jitter.

-All components around the line are potential noise source.



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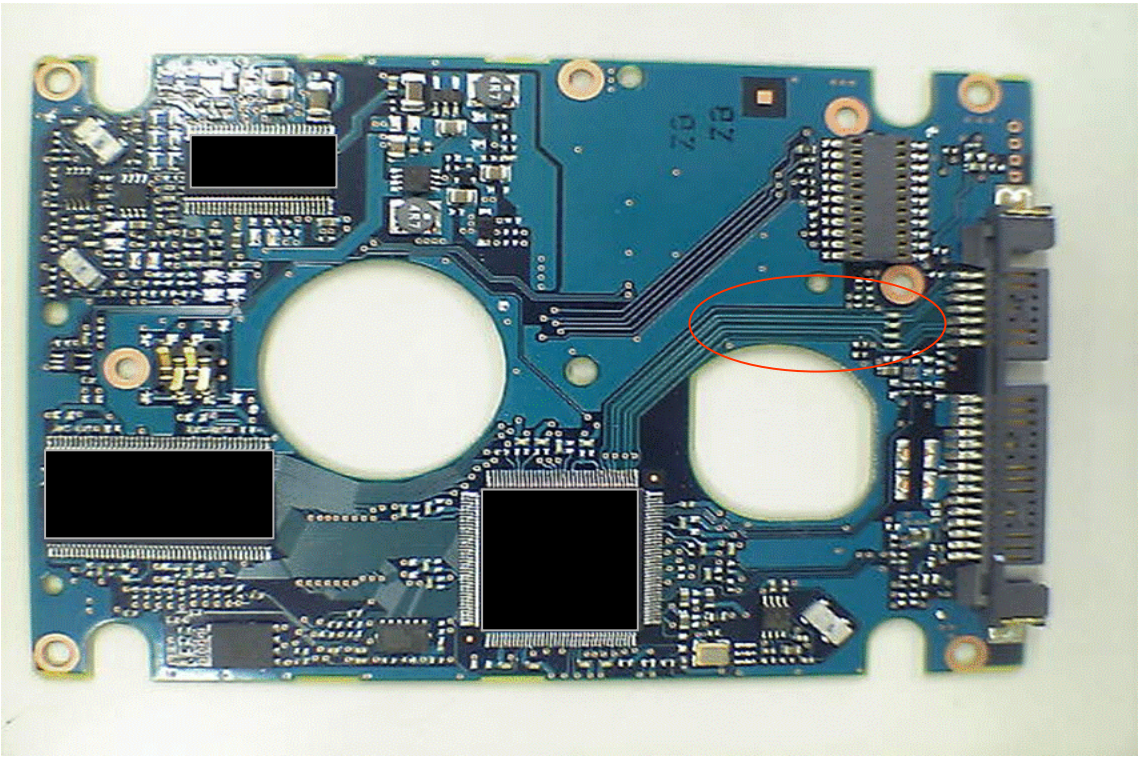
In reality - actual condition is worse than simulation model.



Problem and Solution

One Problem
TX signal for 6 m cable is too strong for 1 m connection
Strong Signal causes Strong Reflection and Cross talk

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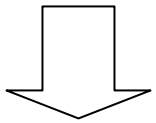
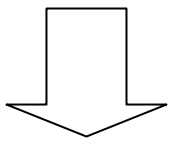


Let's minimize signal strength at RX input on each link

Some RX can operate at lower input signal level than defined

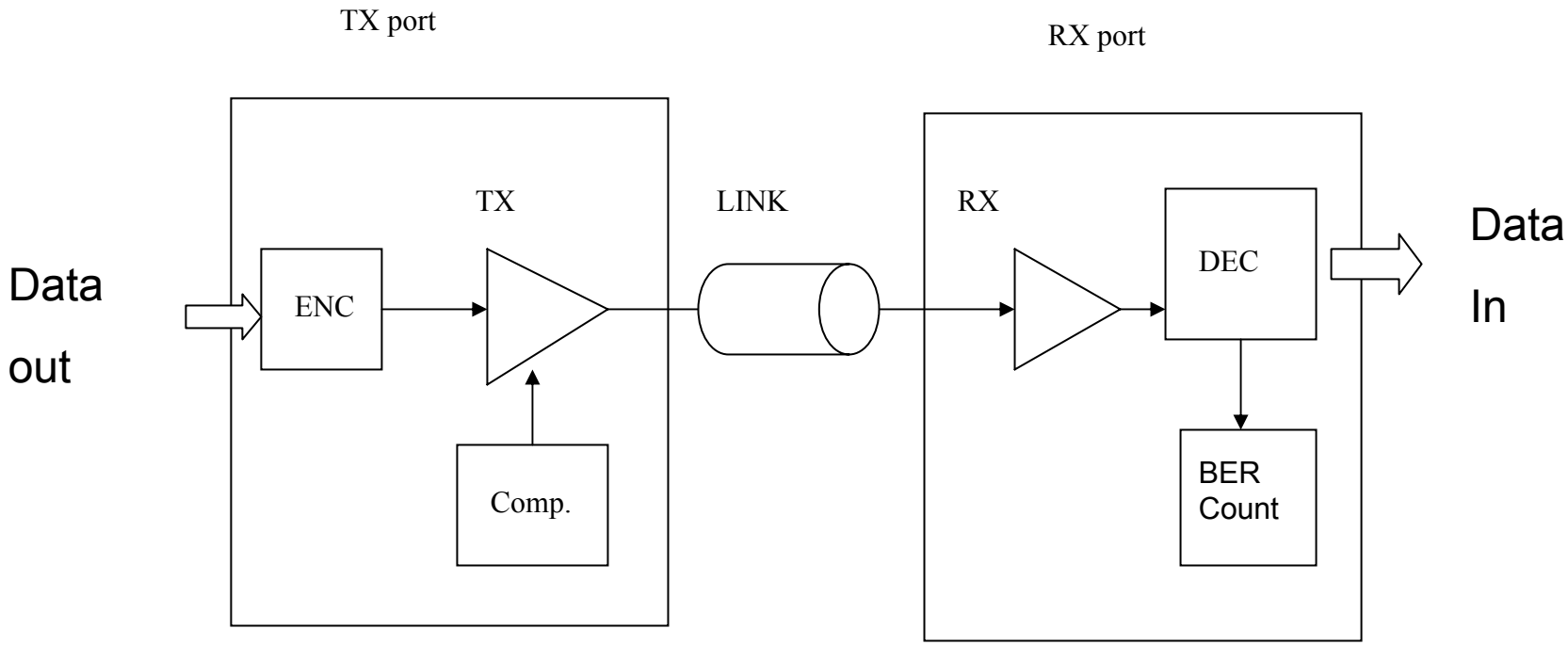


Let's select ideal signal level on each RX

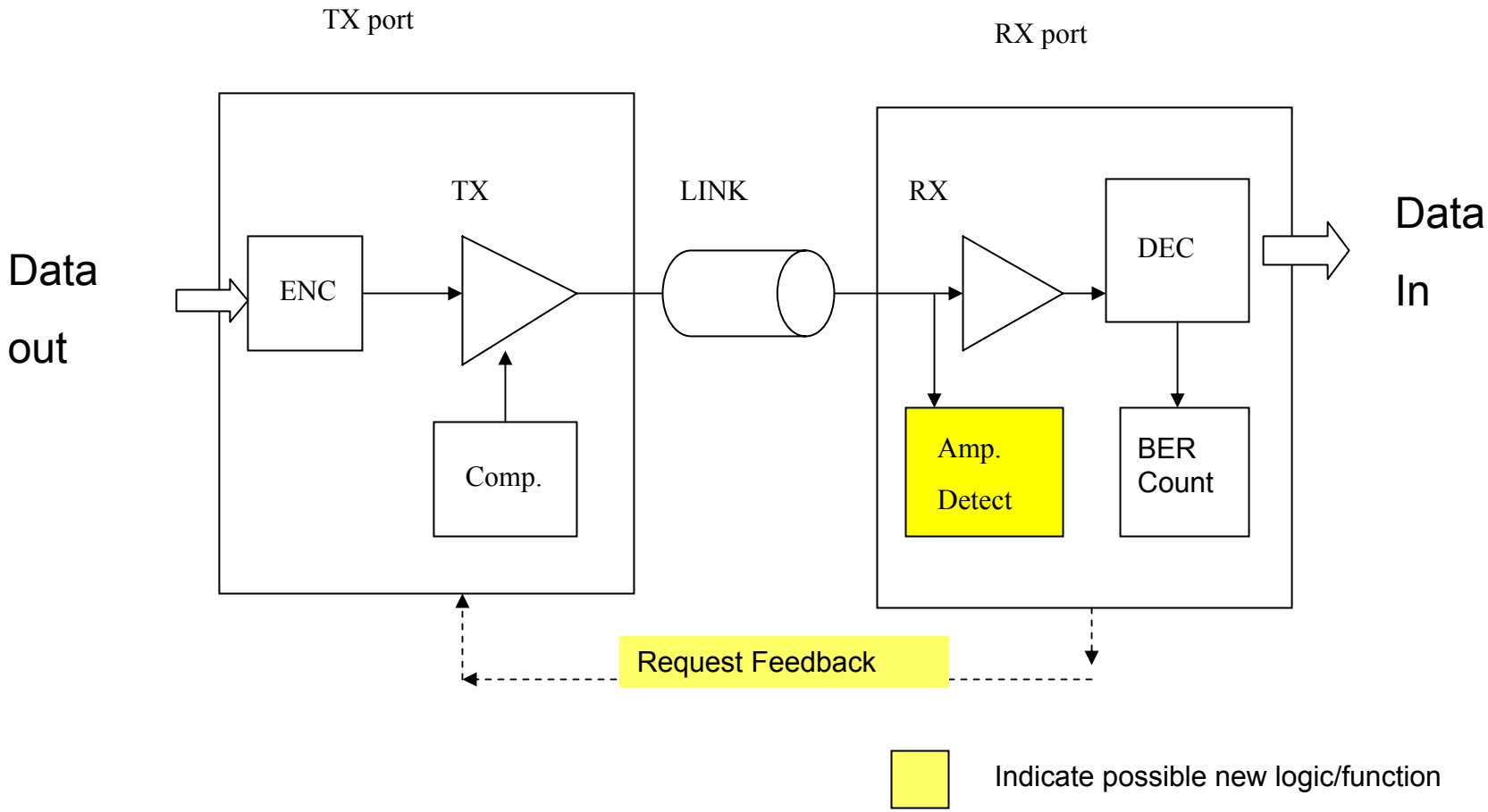
Goal

We can expect more clear Eye Pattern and less Jitter condition

The RX capability can contribute on whole system environment



Simplified concept of System Implementation



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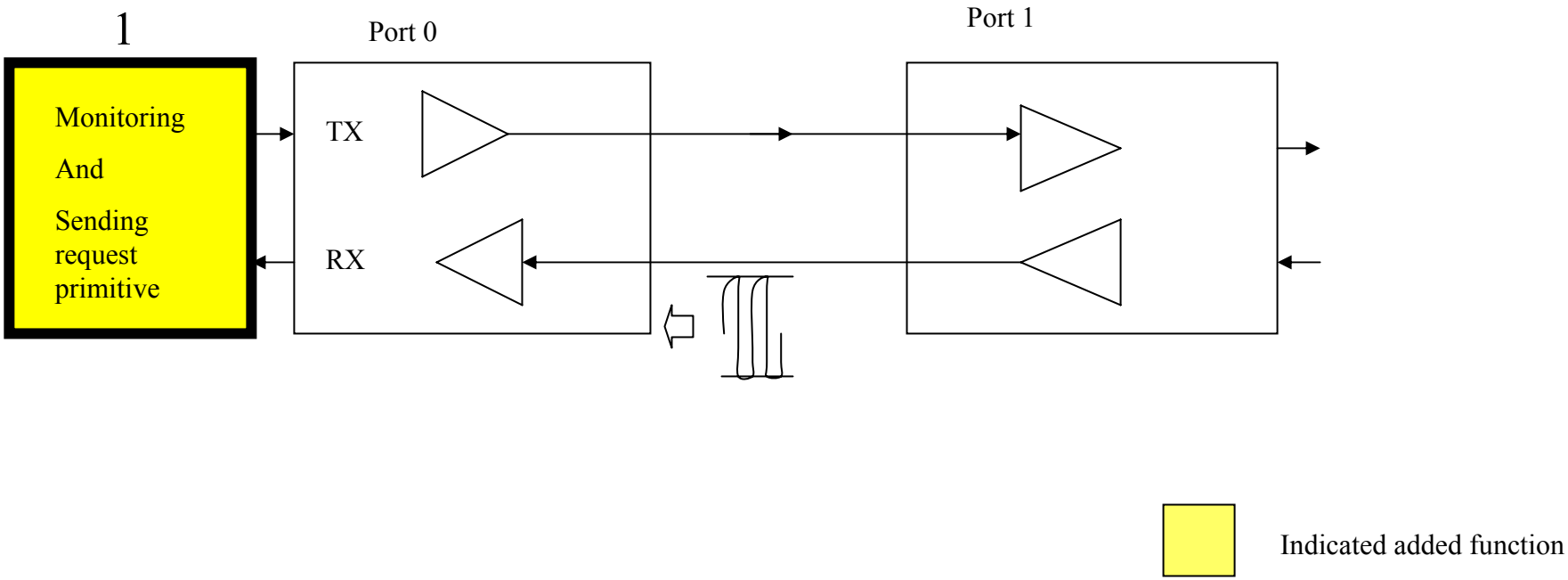
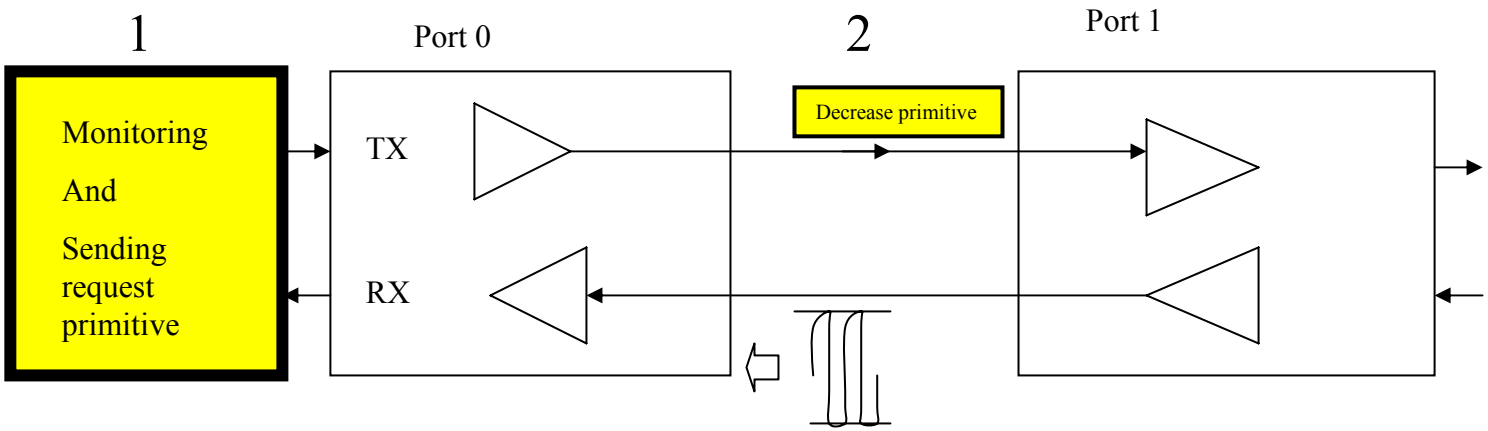


1. Port 0 RX : Monitoring & detecting over level of receiving signal

Scenario of Dynamic Level Compensation



Indicated added function

1. Port 0 RX : Monitoring & detecting over level of receiving signal
2. Port 0 TX : Send Primitive Signal to decrease amplitude level to mate port

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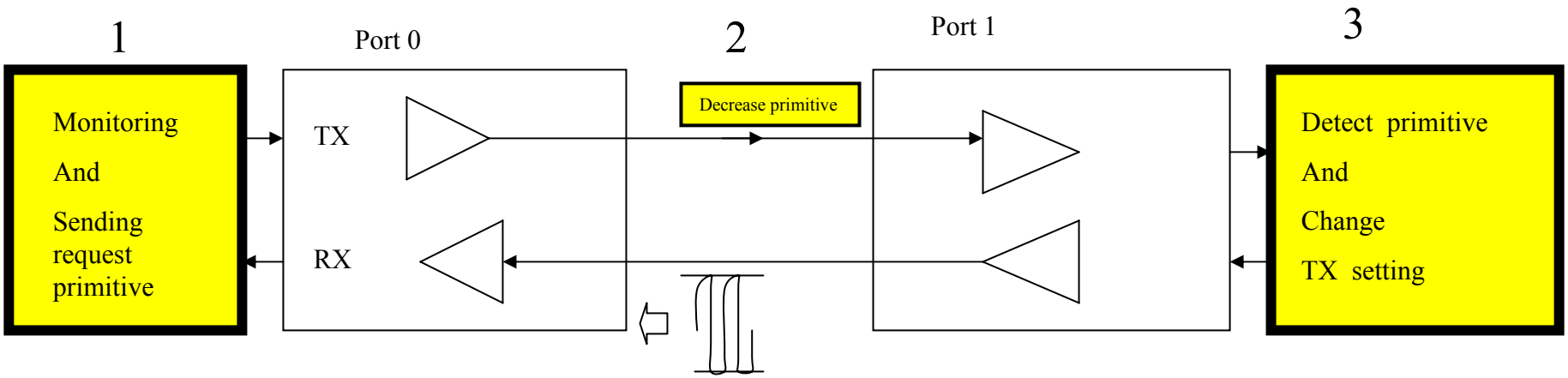

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3. Port 1 RX : Detects Primitive Signal to decrease amplitude

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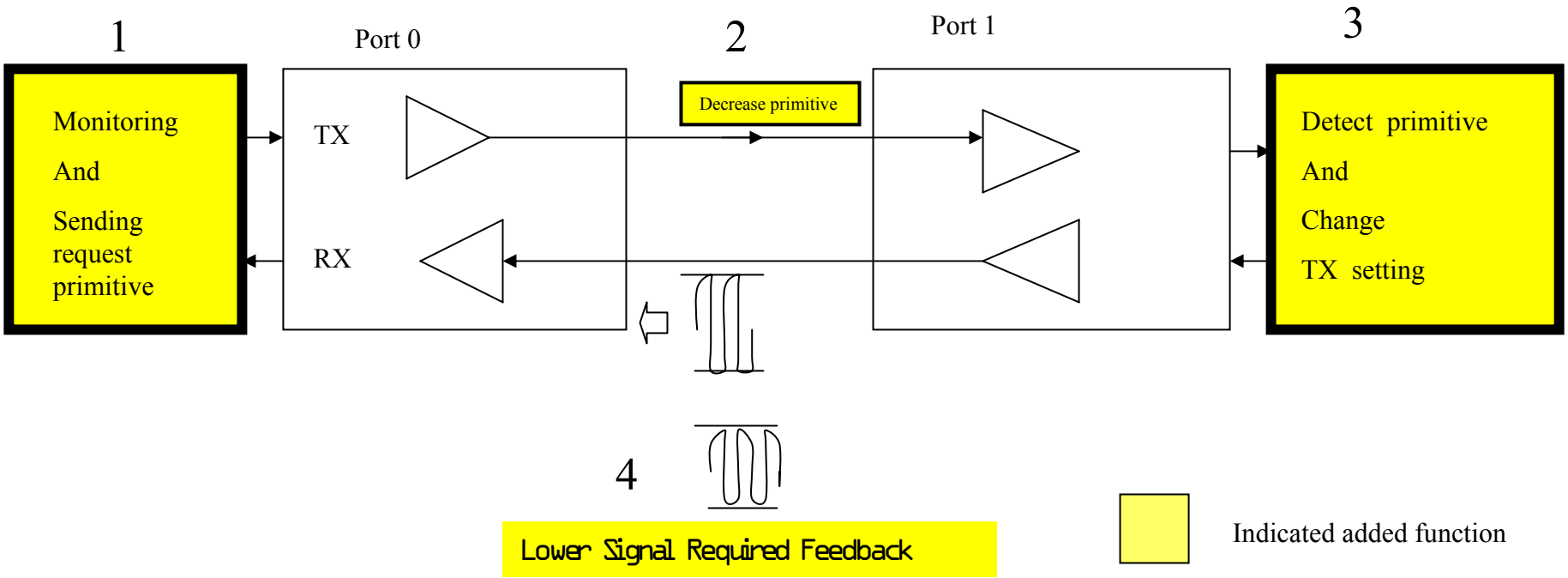

1. Port 0 RX : Monitoring & detecting over level of receiving signal
2. Port 0 TX : Send Primitive Signal to decrease amplitude level to mate port
3. Port 1 RX : Detects Primitive Signal to decrease amplitude
4. Port 1 TX : Decrease TX amplitude & De - emphasis level

The same action can be triggered by Port 1.

Scenario of Dynamic Level Compensation

Parts for Dynamic Compensation

-Input signal amplitude detection circuit - new circuit

-BER monitoring i.e., error counter and frame counter - firmware

-Monitoring change effect and decision logic - firmware or hardware

-Primitive definition i.e., redundant type, increase/decrease - T10 proposal

-Primitive detection circuit - hardware

-TX tune logic i.e., Amplitude/De-emphasis registers - hardware

-Table of parameter value set and pointer logic - firmware or hardware

Need standard definition for Interoperability - T10

Thanks for Reference

-SAS-2 Interconnect Signal-to-Noise Ratio Study (07-484r0)

Barry Olawsky Hewlett Packard

Signal level reduction by cable length and frequency

-Data-Dependent Jitter and Crosstalk-Induced Bounded Uncorrelated Jitter in Copper Interconnects

James Buckwalter, Behnam Analui, and Ali Hajimiri

2004 IEEE MIT-S Digest

Closed link causes Crosstalk which induced uncorrelated Jitter

-SAS-2 Electrical Specification Proposal (06-496r2)

Kevin Witt VITESSE

The signal compensation for frequency and cable length

Many other documents of T10