To: INCITS Technical Committee T10
From: Fred Knight, Network Appliance
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Date: January 15 2008
Subject: SPC4 – Additional Power Management support

1. ***Revision history***
   Revision 0 (14 January 2008) First revision – created from 07-485r0 feedback.
   Revision 1 (15 January 2008) 2nd revision – incorporate feedback from SAT meeting.
   1) Add generic description of ATA Power Condition Page – move specific details to the SAT spec.
   2) Change sub-page number of VU Power Condition page to 0xff.

2. ***Related documents***
   sat2r01a – SCSI / ATA Translation - 2
   spc4r11 – SCSI Primary Commands - 4
   sbc3r11 – SCSI Block Commands – 3
   07-485r1 – SAT-2 Additional power management methods

3. ***Overview***
   The Power Condition Mode Page currently contains an idle timer and standby timer. There are many different type devices (ATA via SAT for example) now using SCSI as its host interface. As a result, the timers in this mode page are insufficient to describe power condition controls necessary for those other interfaces. This proposal is to specifically address the addition of the ATA APM power control value to the power condition mode page.

   This proposal extends the Power Condition Mode Page by adding sub pages for other interfaces. Two sub pages are added. One is added for ATA specific values, and a second for multiple Vendor Unique Timer fields.

Author's notes and comments/questions are seen in blue text (not to be included in the spec itself) and spec changes are in red text.

7.4.12 Power Condition mode page

The Power Condition mode page provides an application client with methods to control the power condition of a logical unit (see 5.9). These methods include:

a) Specifying that the logical unit transition to a power condition without delay; and
b) Activating and setting of idle condition and standby condition timers to specify that the logical unit wait for a period of inactivity before transitioning to a specified power condition.

The mode page policy (see 6.9) for this mode page shall be shared.

When a device server receives a command while in a power condition based on a setting in the Power Condition mode page, the logical unit shall transition to the power condition that allows the command to be processed. If ~~either~~ the idle condition timer, ~~or~~ the standby condition timer, or a VU timer has been set, then they shall be reset on receipt of the command. On completion of the command, the timer(s) shall be started.

Logical units that contain cache memory shall write all cached data to the medium for the logical unit (e.g., as a logical unit does in response to a SYNCHRONIZE CACHE command as described in SBC-2) prior to entering into any power condition that prevents accessing the media (e.g., before a hard drive stops its spindle motor during transition to the standby power condition).

The logical unit shall use the values in the Power Condition mode page to control its power condition after a power on or a hard reset until a START STOP UNIT command setting a power condition is received.

Table 309 defines the Power Condition mode page.

Table 309 – Power Condition mode page

Byte \ Bit	7	6	5	4	3	2	1	0
0	PS	SPF (0b)	Page Code (1Ah)					
1	Page Length (0Ah)							
2	Reserved							
3	Reserved						IDLE	STANDBY
4	(MSB)							
7	IDLE CONDITION TIMER							(LSB)
8	(MSB)							
11	STANDBY CONDITION TIMER							(LSB)

The PS bit, SPF bit, PAGE CODE field, and PAGE LENGTH field are described in 7.4.5.

The IDLE and STANDBY bits specify which timers are active.

If the IDLE bit is set to one and the STANDBY bit is set to zero, then the idle condition timer is active and the device server shall transition to the idle power condition when the idle condition timer is zero.

If the IDLE bit is set to zero, then the device server shall ignore the idle condition timer.

If the STANDBY bit is set to one and the IDLE bit is set to zero, then the standby condition timer is active and the device server shall transition to the standby power condition when the standby condition timer is zero.

If the STANDBY bit is set to zero, then the device server shall ignore the standby condition timer.

If both the IDLE and STANDBY bits are set to one, then both timers are active and run concurrently. When the idle condition timer is zero the device server shall transition to the idle power condition. When the standby condition timer is zero the device server shall transition to the standby power condition. If the standby condition timer is zero before the idle condition timer is zero, then the logical unit shall transition to the standby power condition.

The value in the IDLE CONDITION TIMER field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the idle power condition when the IDLE bit is set to one. The idle condition timer is expired when:

a) The IDLE CONDITION TIMER field is set to zero; or
b) The number of milliseconds specified by the value in the IDLE CONDITION TIMER field times 100 milliseconds has elapsed since the last activity (e.g., processing a command that requires the active power condition or performing a self test).

The value in the STANDBY CONDITION TIMER field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the standby power condition when the STANDBY bit is set to one. The standby condition timer is expired when:

a) The STANDBY CONDITION TIMER field is set to zero; or
b) The number of milliseconds specified by the value in the STANDBY CONDITION TIMER field times 100 milliseconds has elapsed since the last activity (e.g., processing any command or performing a self test).

7.4.12.1 ATA Power Condition Sub-Page

The ATA Power Condition sub-page controls power conditions that are specific to ATA. Table 309B defines the ATA Power Condition sub-page.

Table 309B –ATA Power Condition Sub-Page

Byte \ Bit	7	6	5	4	3	2	1	0
0	PS	SPF (1b)	Page Code (1Ah)					
1	Sub Page Code (01h)							
2	(MSB)							
3	Page Length (12)							(LSB)
4	ATA Specific Parameters							
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The PS bit, SPF bit, PAGE CODE field, and PAGE LENGTH field are described in 7.4.5.

The ATA Specific Parameters are defined in SAT-2.

7.4.12.2 Vendor Unique Power Condition Sub-Page

The Vendor Unique Power Condition Sub-Page contains vendor unique power condition timers.

The interaction between the Vendor Unique timers, as well as the interactions between the Vendor Unique timers and the idle and standby timers is not specified in this standard and are vendor unique. Table 309A defines the Vendor Unique Power Condition Sub-Page.

Table 309A – Vendor Unique Power Condition Sub-Page

Byte \ Bit	7	6	5	4	3	2	1	0
0	PS	SPF (1b)	Page Code (1Ah)					
1	Sub Page Code (FFh)							
2	(MSB) Page Length (28)							
3	(LSB)							
4	Reserved					VUT2	VUT1	VUT0
5	Reserved							
6	Reserved							
7	Reserved							
8	(MSB) VU Timer 0							
11	(LSB)							
12	(MSB) VU Timer 1							
15	(LSB)							
16	(MSB) VU Timer 2							
19	(LSB)							
31	Reserved							

The PS bit, SPF bit, PAGE CODE field, and PAGE LENGTH field are described in 7.4.5.

The VUT0, VUT1 and VUT2 bits specify which timers are active.

If the VUT0 bit is set to zero, then the device server shall ignore the VU TIMER 0.

If the VUT1 bit is set to zero, then the device server shall ignore the VU TIMER 1.

If the VUT2 bit is set to zero, then the device server shall ignore the VU TIMER 2.

The value in the VU TIMER 0 field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the vendor unique power condition 0 when the VUT0 bit is set to one. The VU TIMER 0 condition timer is expired when:

a) The VU TIMER 0 field is set to zero; or

b) The number of milliseconds specified by the value in the VU TIMER 0 field times 100 milliseconds has elapsed since the last activity (e.g., processing a command that requires the active power condition or performing a self test).

The value in the VU TIMER 1 field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the vendor unique power condition 1 when the VUT1 bit is set to one. The VU TIMER 1 condition timer is expired when:

a) The VU TIMER 1 field is set to zero; or
b) The number of milliseconds specified by the value in the VU TIMER 1 field times 100 milliseconds has elapsed since the last activity (e.g., processing a command that requires the active power condition or performing a self test).

The value in the VU TIMER 2 field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the vendor unique power condition 2 when the VUT2 bit is set to one. The VU TIMER 2 condition timer is expired when:

a) The VU TIMER 2 field is set to zero; or
b) The number of milliseconds specified by the value in the VU TIMER 2 field times 100 milliseconds has elapsed since the last activity (e.g., processing a command that requires the active power condition or performing a self test).