T10/07-304r3 Zero-Length Test Load Text SAS-2 Zero-Length Test Load Section

To: T10 Technical Committee
From: Barry Olawsky, HP (barry.olawsky@hp.com)
Date: 4 October 2007
Subject: T10/07-304r3 SAS-2 Zero-Length Test Load Section

Revision History

Revision 0 (3 July 2007) first revision
Revision 1 (10 July 2007) added comments after July 5th conference call. Mostly editorial. Modified equation to allow for VNA calibration tolerance at low frequencies.
Revision 2 (10 July 2007) includes editorial changes made at July 10th face-to-face.
Revision 3 (4 October 2007) includes editorial changes made to Sdd21 equation to accommodate 0.2dB insertion loss at 50MHz.

Related Documents

sas2r10.pdf - Serial Attached SCSI 2 revision
07-013R6 SAS-2 Zero-Length Test Load Characterization (Barry Olawsky, Hewlett Packard)

Overview

Physically implementable zero-length test loads are not ideal. Measurement errors induced by the zero-length test load can be removed by de-embedding although the procedure is not ideal itself. Compliance of fixturing to some performance standards will reduce the measurement error and improve the accuracy of de-embedding.

Suggested Changes

Replace the zero-length test load section with the following text and graphics.

1.1.1.1 Zero-length test load

Figure 105 shows the zero-length test load as used for testing a transmitter device compliance point.

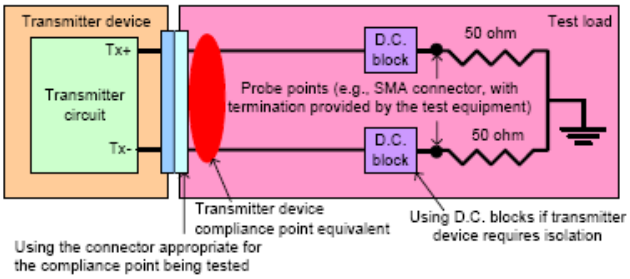

Figure 105 — Zero-length test load for transmitter device compliance point

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Figure 106 shows the zero-length test load as used for testing a receiver device compliance point.

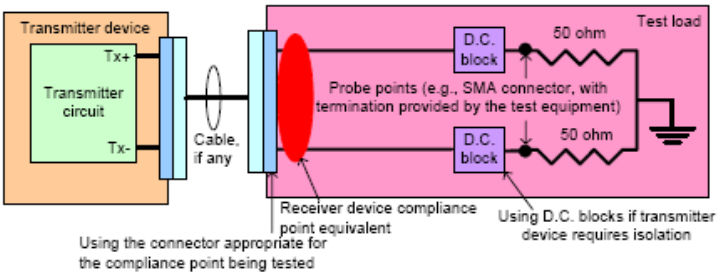

Figure 106 — Zero-length test load for receiver device compliance point

Test loads in a figure 105 and figure 106 show ideal designs. Actual designs include:

- insertion loss between the compliance and probe points; and
- return loss due one or more impedance mismatches between the compliance point and 50 ohm termination points.

Not shown are non-ideal effects of the test equipment raw measurements (e.g., additional insertion and return loss). For de-embedding methods to remove non ideal effects see annex B.

Usage of fixturing and test equipment shall comply with the requirements defined in this subclause. The requirements in this subclause include the combined effects of the fixturing and test equipment.

NOTE: The zero-length test load performance specifications defined in this subclause were not required for previous versions of this standard.

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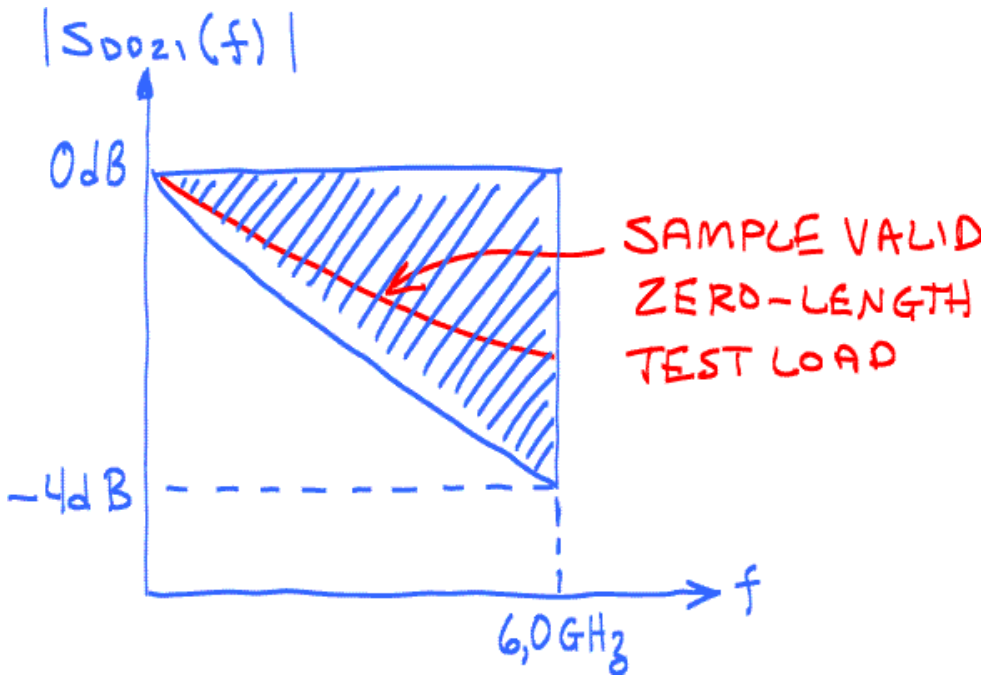

Figure X, Zero-Length Sdd21

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The zero-length test load, including all fixturing and instrumentation required for the measurement, shall comply with the following equations:

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For 50 MHz <= f <= 6,0 GHz:

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$|S_{DD21}(f)| \geq -20 \log_{10}(e) \times ((1{,}0 \times 10^{-6} \times f^{0{,}5}) + (2{,}8 \times 10^{-11} \times f) + (5{,}3 \times 10^{-21} \times f^2)) - 0{,}2$ dB (see figure X)

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$|S_{DD11}(f)| \leq -15$ dB

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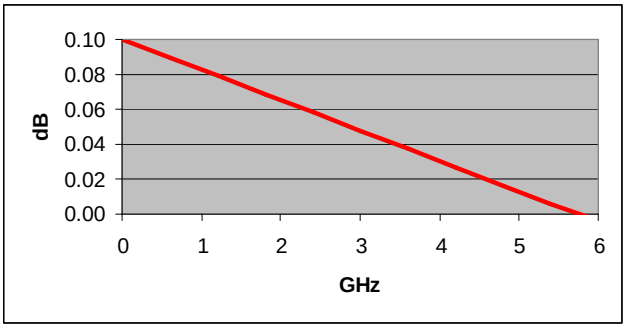
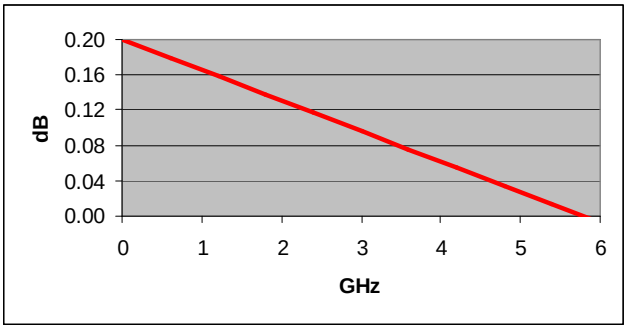
THE FOLLOWING INFORMATION IS DISCUSSION PURPOSES ONLY. IT IS NOT TO BE INCLUDED IN THE SPECIFICATION.

Adding a DC loss of 0.1dB and rescaling the “f” term to “3” to force 4.0dB loss at 6GHz the additional margin is:

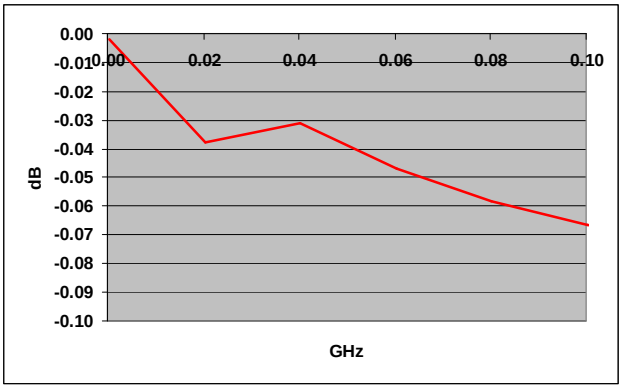


Adding a DC loss of 0.1dB and rescaling the “f” term to “2.8” to force 4.0dB loss at 6GHz the additional margin is:



The original fixture sample data at low frequencies is as follows:

Case 1:



Case 2: