To: T10 Technical Committee
From: Barry Olawsky, HP (barry.olawsky@hp.com)
Date: 10 July 2007
Subject: T10/07-304r1 SAS-2 Zero-Length Test Load Section

Revision History

Revision 0 (3 July 2007) first revision
Revision 1 (10 July 2007) added comments after July 5th conference call. Mostly editorial.
Modified equation to allow for VNA calibration tolerance at low frequencies.

Related Documents

sas2r10.pdf - Serial Attached SCSI 2 revision
07-013R6 SAS-2 Zero-Length Test Load Characterization (Barry Olawsky, Hewlett Packard)

Overview

Physically implementable zero-length test loads are not ideal. Measurement errors induced by the zero-length test load can be removed by de-embedding although the procedure is not ideal itself. Compliance of fixturing to some performance standards will reduce the measurement error and improve the accuracy of de-embedding.

Suggested Changes

Replace the zero-length test load section with the following text and graphics.

1.1.1.1 Zero-length test load

Figure 105 shows the zero-length test load as used for testing a transmitter device compliance point.

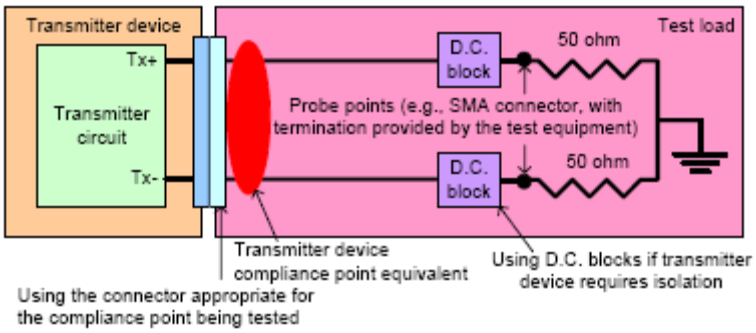


Figure 105 — Zero-length test load for transmitter device compliance point

Figure 105 — Zero-length test load for transmitter device compliance point

Figure 106 shows the zero-length test load as used for testing a receiver device compliance point.

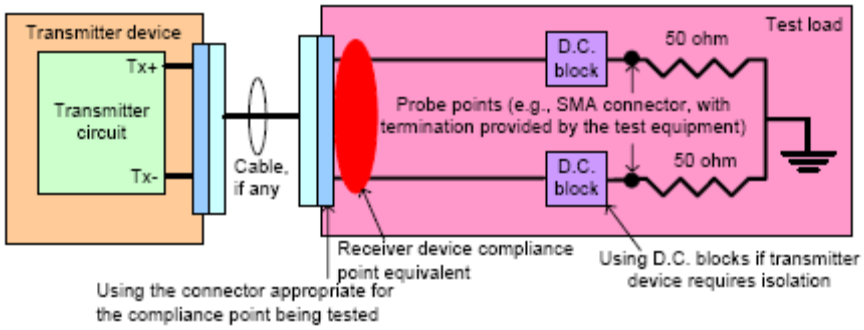
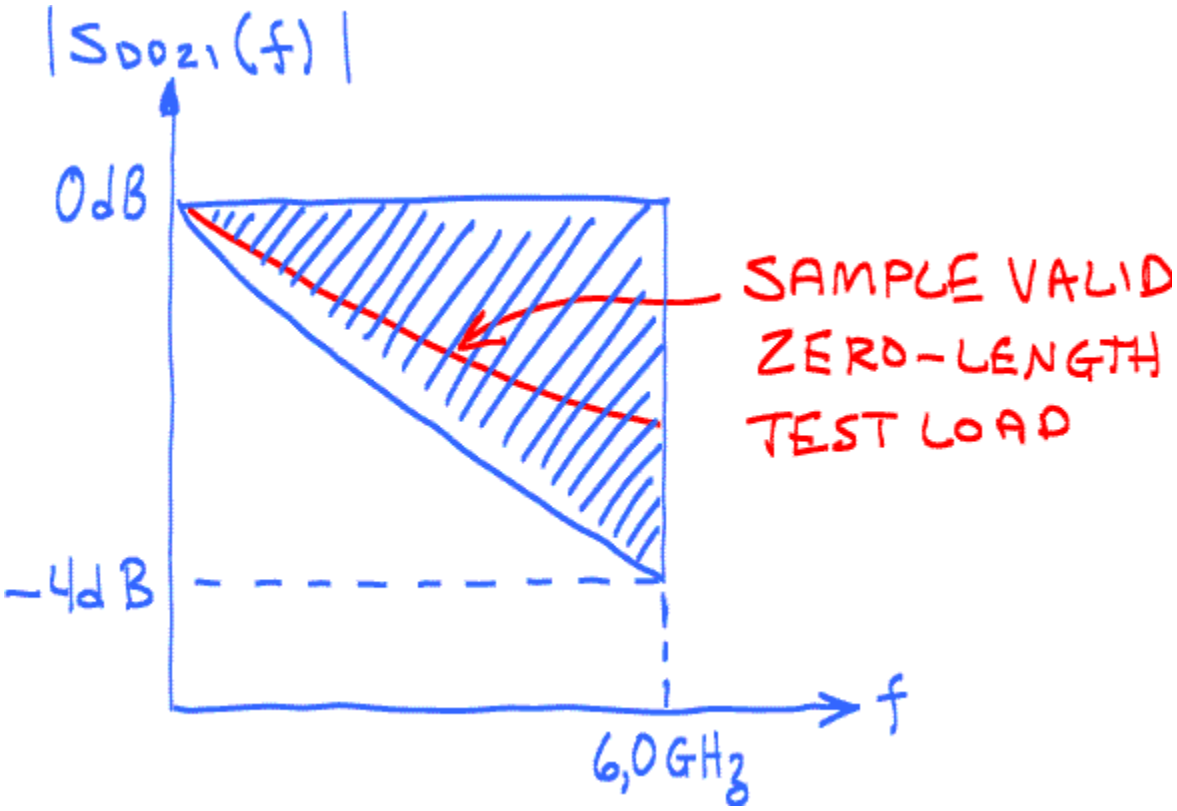


Figure 106 — Zero-length test load for receiver device compliance point

Test loads in a figures 105 and 106 show ideal designs. Physically implementable designs include insertion loss between the compliance and probe points and return loss due one or more impedance mismatches between the compliance point and 50 ohm terminations points. Also not shown are non-ideal effects of the test equipment such as additional insertion and return loss. Refer to Annex B for de-embedding methods to remove such effects.

Since the de-embedding process can be difficult to perform accurately, usage of fixturing and test equipment that complies with the following specification is recommended. This specification applies to the combined effects of the fixturing and test equipment. The following zero-length test load performance specifications apply.



The zero-length test load (including all fixturing and instrumentation required for the measurement) shall comply with the following equations:

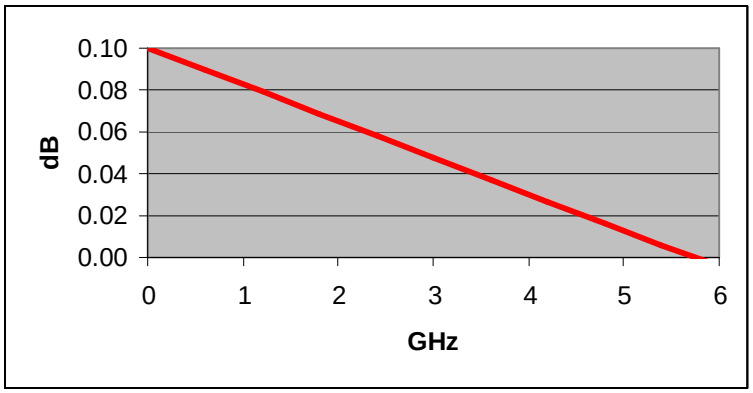
For 10 MHz <= f <= 6,0 GHz:

$|S_{DD21}(f)| <= -20 \log_{10}(e) \times ((1{,}0 \times 10^{-6} \times f^{0{,}5}) + (3{,}2 \times 10^{-11} \times f) + (5{,}3 \times 10^{-21} \times f^{2}))$ dB

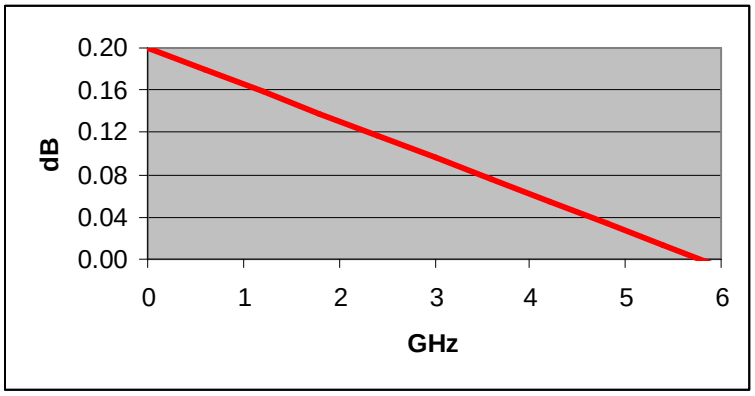
$|S_{DD11}(f)| >= -15$ dB

THE FOLLOWING INFORMATION IS DISCUSSION PURPOSES ONLY. IT IS NOT TO BE INCLUDED IN THE SPECIFICATION.

Adding a DC loss of 0.1dB and rescalling the “f” term to “3” to force 4.0dB loss at 6GHz the additional margin is:

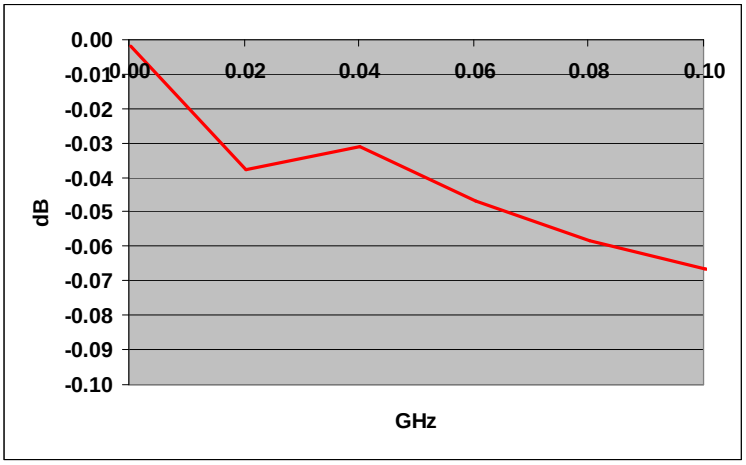


Adding a DC loss of 0.1dB and rescalling the “f” term to “2.8” to force 4.0dB loss at 6GHz the additional margin is:



The original fixture sample data at low frequencies is as follows:

Case 1:



Case 2: