Improving a Jitter Definition

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Introduction

This presentation has been regenerated and reorganized from selections of presentations given to the SATA-IO PHY Working Group in December 2006 through April 2007. The numerical examples are based on the present SATA Gen2i Jitter Definition, but the general concept may be applied to any Serial Data Standard, that derives their Jitter Definition from a recovered clock or reference clock characteristics. Using the numerical examples from the SATA Gen2i Jitter Definition provides a more concrete example of the concepts being presented. This provides more clarity than presenting only the general concepts.

This presentation is being released into the public domain such that other industry experts may evaluate and improve on the concepts in order to advance the general industry. (be free!)

Serial Data Jitter Background

- To insure interoperability between serial data transceivers many parameters need to be controlled with the appropriate budgets. Transmit (TX) jitter and Receive Jitter Tolerance (RXJT) are two key parameters that need to be controlled properly to achieve the interoperability goals.
- To properly control these jitter parameters, the definition of what is considered jitter, and an accurate means of measuring the jitter are both required. This becomes even more important as the data rates increase and the resulting timing budgets decrease.
- With the inclusion of Spread Spectrum Clocking (SSC) the differentiation between what is allowable timing variation and what is considered jitter becomes very critical.
- This presentation provides a direction to improve the method of defining this boundary between jitter and allowable timing variations, and by doing such better controls the compliance of transceivers. Additionally this method allows for verifying the characteristics of the Jitter Measuring Devices (JMDs) that are used to test this compliance.

Scope of This Presentation

- Experts in the field of serial data communications have long experienced the uncertainty caused by differences in the reported jitter values made by various JMDs. Part of this is due to the lack of clarity in the particular Standard's Jitter Definition, which may cause various interpretations of the Jitter Definition by the PHY designers and JMD manufacturers. Other possible variations in JMDs reported jitter levels may be due to the jitter extraction algorithms and hardware. Some of the possible differences between JMDs are:
  - Jitter component separation methods
  - Timing and capture hardware differences and methods
  - Total jitter (TJ) calculation or estimation methods
  - Size of the population of timing events used to estimate the TJ.
  - The method of differentiating jitter versus allowable timing variations
- This presentation focuses on the last of these possible differences primarily by improving the Jitter Definition method that controls this differentiation.
- The general goal, using the examples provided, is to transform a present Jitter Definition method into a more clear and defining method of specifying the Jitter Definition such that the interpretations are more uniform, and the characteristics of the JMD being used to verify compliance to the serial data standard may be easily verified.

A Quote: A man with one JMD always know his jitter, a man with two or more JMDs is never quite sure. – adapted by JH

Presentation Overview

- **Section 1:** A look at present Jitter Definition methods as are being used in several standards.
- **Section 2:** An overview of PLL terminology and characteristics, along with a discussion of possible misconceptions that may be present.
- **Section 3:** Shifting to a New Jitter Definition Method
- **Section 4:** JTF Verification Method
- **Section 5:** An Improved Jitter Definition Specification Example

Section 1

First, a look at Present Jitter definitions and what they really infer.

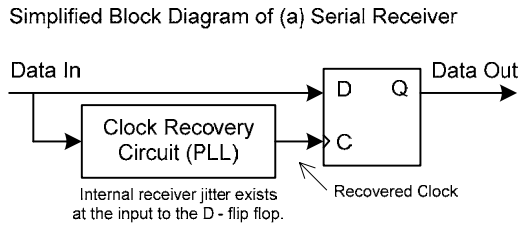
SATA Rev 2.5 Jitter Definition

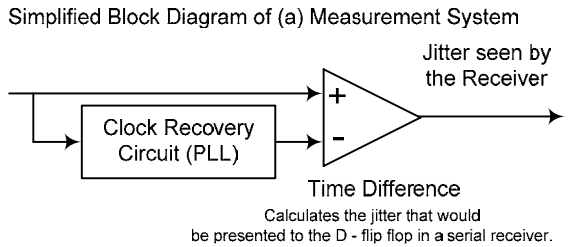
A Present Spec, For an Example.

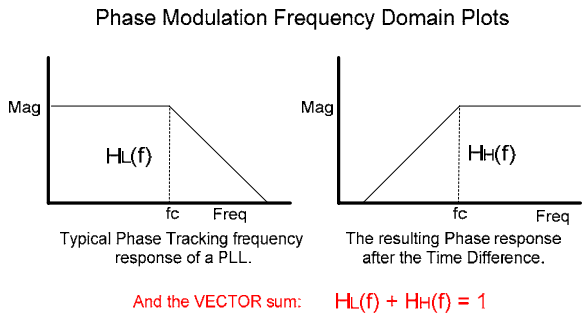
- Jitter is the short-term variations of the zero crossings from ideal positions in time. A "Reference Clock" (defined in section 7.3.2) defines the ideal positions in time. *(Sec 7.3, p 185)*
- The Reference Clock definition (Sec 7.3.2, p 186) states:
  - Reference clock extraction is performed using either hardware or software PLLs.
  - The PLL is Type 2.
  - The -3dB corner frequency is fb/N. (at present for Gen2i, N = 500 &10, Genx = 1667)
  - This corner frequency is exhibited by the PLL for a pattern with a transition density (Dt) of 1.0 (a clocklike pattern 1010…) and a damping factor (z or zeta) of 0.707 min to 1.000 max.
- Jitter Measurements (Section 7.4.7, p 214) further states:
  - The BERT scan method described in section 7.4.7.1 is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. (Direct measurement to a BER 1E-12)
  - The clock recovery circuit has the defined low pass function H_L. The time difference between the reference clock and the data, results in a high pass function H_H. The resulting jitter seen by the receiver has the high pass function H_H. **This defines the measurement function required by all jitter measurement methodologies.**

Present Jitter Definition Concepts

- The top diagram gives a view of one type of receiver topology, showing where the jitter affects the quality of the data recovery.
- The second diagram show a system that reports the jitter that the receiver would see if the CR response is the same as the receiver CR response. (a measurement system should emulate this)
- The frequency domain plots show how the PLL has a low pass function, and the resulting output of the time difference is a high pass function.
- The most important thing on this slide is the equation that relates these two functions. The Vector Sum requires that phase as well as magnitude must be considered. (The fc in the first plot is not the fc in the other plot!)







At first glance, one could erroneously assume that the CR plus time difference could be replaced by a High Pass filter with the same fc as the PLL fc. There is more to it than that, due to the phase characteristics of the PLL.

The Present Jitter Definition

- One intent of this description is to specify what is considered as jitter and what are allowable timing variations. This differentiation is controlled by the characteristics of the Clock Recovery or PLL specified in the associated standard.
- Another intent, is for the PLL in the measurement system to have the same characteristics as the PLL in the receiver, such that the jitter reported by the measurement system reflects what is seen in the receiver. How this PLL is specified, makes the difference between a clear Jitter Definition and one that can be erroneously interpreted.
- Allowing multiple interpretations, results in varying reported jitter from multiple JMDs, and can lead to reduced margins in combined serial communication systems in which communicating transceivers have been checked for TX Jitter and RXJT using different perceived Jitter Definitions. As data rates increase, tighter tolerances on the jitter (definition and measurement) are a necessity.
- Since there is a multiplicity of receiver types, the simplified receiver and clock recovery or PLL is intended to be a reference. All who develop proprietary architectures different than the reference design (as is often the case) are responsible for the proper margins to insure operation of their receiver if the jitter, as defined by the reference receiver and measured by the equivalent JMD, is applied.
- Earlier Jitter Definitions called out a Type 1 PLL since the reference receiver and measurement systems did not have to reject Spread Spectrum Clocking (SSC). Now that SSC is used in many systems, a Type 2 or equivalent PLL needs to be used. This adds more degrees of freedom in the design, and results in more variation from unit to unit, depending on how the PLL characteristics are specified.

Section 1 Key points

- Present standards use closed loop parameters of a PLL to define what is considered jitter and what is considered allowable timing variations.
- There can be misinterpretations in how the “High Pass function” after the time difference, relates to the “Low Pass function” of the PLL.
- A clear jitter definition is required to minimize differences in reported jitter levels, such that interoperability can be improved.
- A JMD should emulate the reference design, such that the reported jitter is equivalent to what the reference receiver would “see”.
- As data rates increase and systems contain SSC modulation, the differentiation between what is considered jitter and what is to be considered as allowable timing variations becomes more important.

Section 2

Since the Jitter Definition is controlled by the characteristics of a PLL, it is important to understand some PLL terminology and characteristics .

Present Jitter Definitions may consist of a mixture of open loop and closed loop PLL characteristics, that depending on interpretation, may result in different measurement methods and results. In some cases, the requirements pose unnecessary constraints, and miss the intended purpose of the definition. In other cases, the specified characteristics do not sufficiently control the desired response.

In order to provide a background for understanding of the Jitter Definitions, the following slides provide a brief look at the terminology and underlying meanings. This will aid with the evolution to an improved Jitter Definition.

So let's look at the Jitter Definition Facts and Fiction.

Jitter Definition Facts and Fiction

1. A type 2 PLL defines that there are two poles at the s-plane origin of the open loop transfer function. (two integrations in the loop) [FACT]
2. A type 2 PLL infers that the asymptotic high frequency roll off is -40dB/dec. [FICTION]
3. A damping factor of 0.707 to 1.000 totally defines no magnitude peaking in the closed loop response of a PLL. [FICTION]
4. A second order HPF is equivalent to a PLL high pass jitter tracking error TF with the present definition. [FICTION]
5. If one tries to measure jitter using a HPF (see #4), the CLTF corner frequency (fc) of the jitter definition PLL should be used as the corner frequency of the HPF. *(this is somewhat irrelevant since a HPF does not provide the correct response with this definition, and should not be used.)* [FICTION]
6. The HF asymptotic roll off of the PLL closed loop transfer function somehow relates to the PLL tracking capability (High Pass function) of the jitter definition. [FICTION]

Lets look at the fictional assumptions in more detail.

Fictional Assumption #2

- Having two poles at the origin (Type 2) does not define the "order" of the system (number of poles in the CLTF) or the asymptotic HF roll off rate. The difference between the number of zeros and the number of poles in the CLTF determines this roll off rate. (sometimes referred to as the "pole excess") For example: If the compensator block in the loop is a PI (Proportional+Integral) controller, the Type 2 PLL will be second order and will have a -20 dB/dec HF CLTF roll off. If the compensator block is an integrator plus a lead compensator (1 pole &1 zero), the Type 2 PLL will be third order and will have a -40 dB/dec HF CLTF roll off. Both are stable and Type 2, but have different closed loop characteristics. This assumes a continuous, linear PLL, with no added parasitic effects included. (a simple model) Today's PLLs can be more complex and still be Type 2. What really is important for our jitter definition, is the gain and phase of the OLTF at the frequencies of interest, not the resulting CLTF. The Jitter Transfer Function (JTF) produced due to the OL Gain and phase is the real target we are trying to define.

One point here, is that it is not sufficient to state "Type 2 PLL" to try to describe the roll off characteristics of the closed loop response. Additionally, requiring a "Type 2 PLL" over constrains the PLL design choices. A "Type 1 PLL" (by the definition) could provide the same SSC Tracking capability as a " Type 2 PLL". A true Type 1 PLL would not have enough OL gain at lower frequencies to properly track SSC. What is really important is the PLL tracking error or JTF for frequencies of interest.

Fictional Assumption #3

- Specifying the zeta of the complex pair of poles in a PLL CLTF, does not totally control the peaking in the closed loop response. The compensation in the loop dominates the dynamics in the loop and therefore the peaking. The pole-zero locations of the compensation have major effects on the CL response. (that is why they exist) Alternatively, the zeta in a second order HPF does control the peaking, since this is formed by a single complex pole pair. For this HPF, a zeta of 0.707 to 1.000 prevents any peaking in the CLTF. (But the jitter definition is not a 2nd order HPF) Zeta is a valid parameter for one class of PLLs (TYPE I, Second Order) but for a Type II PLL a zeta of 0.707 to 1.000 actually forces peaking in the CLTF.
- Since our PLL is a sampled data system, the ratio of the sampling rate (a function of data rate and transition density) to the bandwidth (actually wn) also effects the gain-phase margin in the open OLTF and therefore the peaking in the CLTF. Once again, what is important to the jitter definition is the gain and phase of the OLTF at the frequencies of interest which defines the JTF (or Tracking Error).

In a PLL, specifying zeta is not sufficient to describe the peaking in the closed loop response. Alternatively, we need to focus on the tracking error (or JTF) of the PLL to better define the jitter definition. This is what is important. The closed loop response is modified by changes in the open loop characteristics, but this could be considered secondary to the jitter definition goal. Peaking in the CLTF does not equal peaking in the Tracking Error response. The -3dB frequencies are also different.

Fictional Assumptions #4 and #5

- Processing jitter data with a second order HPF, with a zeta = 0.707 to 1.000, and a corner frequency of the PLL fc is not a valid substitution for the PLL jitter definition, for the following reasons:
  - The Dt (Transition density) of the pattern changes the BW and jitter tracking error of a PLL, but a HPF BW remains constant. If we specify the BW of a PLL at a Dt of 1.0, but the 8b10b encoded data has a Dt of 0.5 on average, the actual BW of the PLL is about half, or less, of the specified value during a jitter measurement. (if no Dt compensation mechanisms are present)
  - The Dt of the pattern changes the magnitude of the peaking in the CLTF of the PLL but does not affect the HPF. This change of peaking in the PLL CLTF, is an indicator that the gain and phase of the OLTF has changed, and therefore the jitter tracking error is also changing. PLLs with different OLTF characteristics with have different peaking changes with changes of Dt.
  - The phase margin and loop gain, and therefore the jitter response and the closed loop response of a PLL, is altered greatly as a function of the Dt of the pattern, even more if the sample rate (transition rate) is not much-much greater that the BW of the PLL. A HPF response does not mimic these characteristics contained in our jitter definition.
  - The -3dB frequency of the high pass function JTF of a PLL may be at 1/2 to 1/4 of the -3dB frequency of the low pass function of the CLTF. The ratio depends on the gain and phase of the open loop characteristic. When we specify a PLL CLBW of 6 MHz, the JTF may have a -3 dB frequency in the area of 1.5 MHz to 2 MHz. Obviously post processing jitter data with a second order HPF with a -3 dB frequency of 6 MHz has different jitter component weighting. (Data will be shown later.)

A second order HPF is not a substitute for a PLL jitter tracking error definition. For a fixed Dt a substitution would be possible, but the -3dB corner frequency would have to be set at a different frequency than the CLTF -3dB BW of the PLL.

Fictional Assumption #6

- The HF asymptotic roll off of the PLL closed loop transfer function does not directly relate to the PLL tracking capability (High Pass function) of the jitter definition. (also known as JTF or jitter transfer function)
  - The closed loop HF roll off occurs at frequencies above the OL unity gain crossover point (GH =1) of the open loop response. In this frequency range, there is no longer any tracking capability achieved by the loop. The shape and slope of the CL roll off, is totally determined by the forward path gain G(s) at those frequencies.
  - At frequencies lower than the open loop unity gain crossover, the loop is active and the closed loop response is usually approximated to be constant. (not actually) The tracking capability or conversely the tracking error is determined by the loop gain. It is impractical to deduce this capability by closed loop measurements in this frequency region. (-0.09 dB vs -0.009 dB is seen in the CLTF for an open loop gain change of 40 dB to 60 dB.)
  - These two frequency regions can be considered to be somewhat independent. Specifying the closed loop roll off, does not define anything about the low frequency tracking capability, as might be inferred by simple inspection of the jitter definition diagrams shown in the specification.

This is a simplified view of loop operation presented to provide insight.
Details in the slides that follow will make this more clear.

So let's examine the differences between the Closed Loop Transfer Function (CLTF) and the Jitter Transfer Function (JTF)

JTF versus CLTF

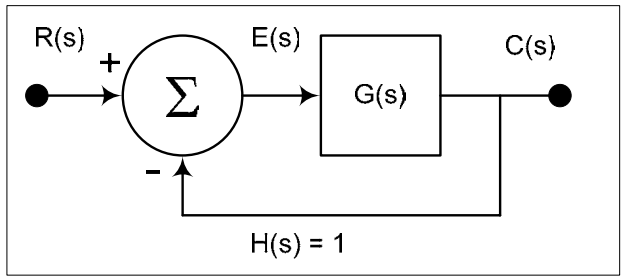
By inserting the generic model of a clock recovery circuit into the SATA specification figure, one can see that E(s) or Tracking Error, is what our jitter definition is defining. [E(s) = R(s) – C(s)] The JTF defines the magnitude and phase of the the “Jitter seen by the Receiver” E(s) compared to the Jitter in the input signal R(s).

E(s) is determined by the open loop gain and phase at frequencies below the unity gain crossover. The observable/measurable Closed Loop response is only available for frequencies near and above the unity gain crossover.

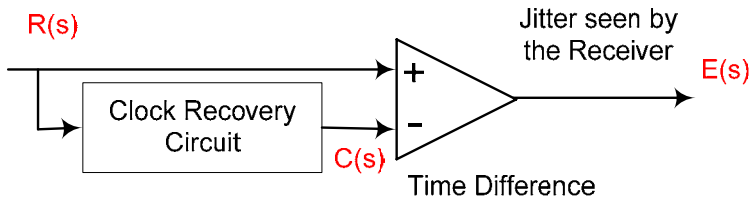
Depending on G(s), these two regions can be quite independent. Specifying the measurable Closed Loop response, does not totally define the Tracking Error.

It can be seen in the CLTF equation that if G(s) is much greater than 1 (when the CR is tracking the jitter) almost any G(s) (allowable by stability constraints) looks like any other G(s). On the contrary, the JTF can be very different, depending on G(s). When G(s) is much greater than 1, JTF is the inverse of G(s).

This is why defining a CLTF does not correlate to an unique JTF. In the present SATA specification, we have clearly called out a jitter definition based on the JTF, but have tried to define it with closed loop BW and a “zeta” that was intended to control peaking.



(Generic Clock Recovery Circuit)



(From Fig 117, page 215, of the Rev 2.5 SATA Spec.)

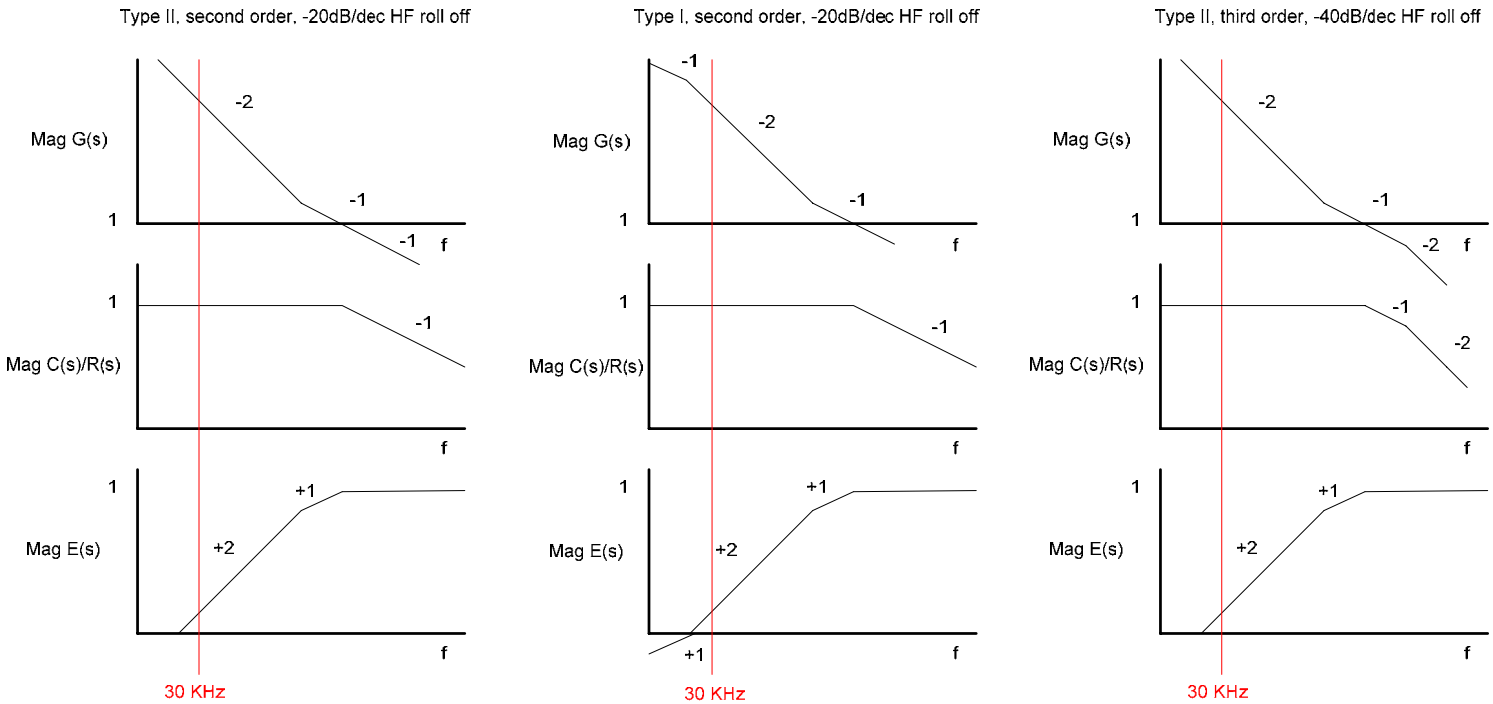
Red Text Added to original Fig

$$JTF = \frac{E(s)}{R(s)} = \frac{1}{1 + G(s)} \qquad CLTF = \frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)}$$

Equations valid for unity gain feedback: H(s) = 1

Jitter Definition Discussion

Looking at simplified Bode Plots of the variables of the generic Clock Recovery system, one can see the effects of the Open Loop Gain on the Closed Loop Gain and the Tracking Error. Note that for all these types of loops the Open Loop Gain and the Tracking Error is the same at the fundamental and harmonics of the SSC. (Mag. only)



The top row is the Open Loop Gain. The middle row is the Closed Loop Gain. The bottom row is the Tracking Error or JTF. The idealized slopes are coded as: -1 = -20dB/dec, -2 = -40 dB/dec, +2 = + 40 dB/dec…

The SSC tracking capability of all these loops are the same. (different Types, orders, and HF roll offs.)

CLTF versus JTF

- In the simplified Bode Plots it can be seen that the Closed Loop response (CLTF) and the Jitter Transfer Function (JTF) or Tracking Error are not directly correlated. BW and peaking are different as well as the roll off rates.
- One must consider the phase of the loop variables to understand why the CL transfer function can have magnitude peaking, while the JTF may not have magnitude peaking. (or the other way is possible)
- For a unity feedback system (H(s)=1) the CLTF = G(s)/[1+G(s)] and the JTF =1/[1+G(s)], where s = jw for sine wave frequency response. Phase is important. (1 is a mag. of 1 at an angle of 0 degrees, all calculations are performed using vector math.)
- When G(s) is very large compared to 1, the CLTF is approximately 1 and the shape of the OL magnitude and the phase cancel. But in the case of the JTF or Tracking Error, a large G(s) makes the error smaller, and the phase is just inverted.
- Near the unity gain region (G(s) = 1) the CLTF and JTF deviate more when considering the vector 1@0deg in the equations. We are attempting to define the JTF by specifying BW and Peaking in the Closed loop response in the present SATA spec. There are many JTFs that can create the same CLTF. When you measure jitter with a JMD, your measured values are weighted by the JTF.

The point here, is that making definitions based on the CLTF does not define a unique JTF, so JMDs can measure different amounts of Jitter from the same source and have the same CLTF. (This is one reason for different pieces of test equipment measuring different amounts of jitter.)

Comparison of CLTF and JTF CR Characteristics

This table shows the BW and peaking of the CLTF and JTF of several practical CR designs. Some are hardware and other are simulations. Most are Type 2, or equivalent OL gain, at frequencies 30 KHz and above. (the example with 0 JTF peaking is a Type 1)

CLTF BW (MHz)	CLTF Peaking (dB)	JTF BW (MHz)	JTF Peaking (dB)	BW Ratio JTF/CLTF (#)	PK Ratio JTF/CLTF (#)
8.8	2.1	2.0	4.1	0.23	1.93
6.5	1.6	2.9	1.2	0.45	0.77
6.8	2.2	1.9	3.7	0.28	1.66
9.2	1.0	2.3	4.1	0.25	4.13
6.9	1.1	2.2	4.7	0.32	4.23
10.1	0.2	2.6	4.1	0.26	20.65
6.1	1.2	3.9	0.0	0.64	0.00
7.0	0.2	2.5	3.6	0.36	18.15

The last two columns calculate the ratios of the -3 dB BW and peaking for the JTF and the CLTF. It can be seen that there is a lot of difference in these ratios. This depends on the design's chosen open loop characteristics.

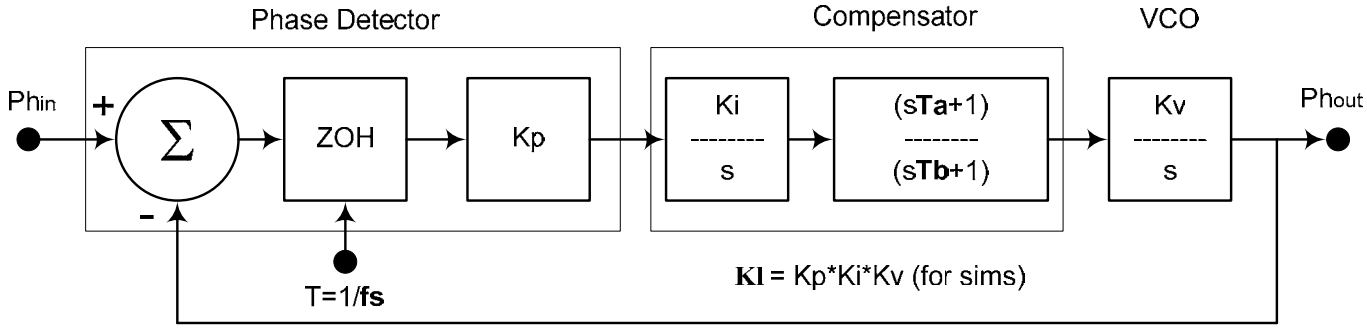
At present we specify a CLBW of 6 MHz for fb/500. This actually represents a JTF BW in the range of 1.4 MHz to 2.7 MHz for the designs above. Post processing with a second order HP filter with a BW of 6 MHz is not equivalent to our present definition.

In order to validate the simplified bode plot asymptotic views of different types of loops shown previously, simulations of two example PLLs are presented.

Example 1 is a Type 2 PLL and Example 2 is classified as a Type 1 PLL (single integration in the OLTF) but has a low frequency real pole in the OLTF that provides the same gain and phase of the OLTF at SSC frequencies.

Caution, a pure Type 1 PLL would not be valid in a system with SSC modulation!

Example 1 Clock Recovery System



- This CR example is a Type II, third order PLL with a -40 dB/dec HF roll off.
- Other internal implementations are possible, but for analysis, a generic structure has been chosen.
- Note that the phase detector gain (Kp) has been made constant, as a function of RL (Run Length) to observe only the effects of the ZOH. In practice this will also vary with Dt, causing changes in open loop gain, closed loop BW and peaking.
- For Reference, the resulting optimized parameters are provided:
  - Fb/500: Kl=1.76E14, Ta=1.43E-7, Tb=7.14E-9

Before simulating, lets look at the basic effects of the Zero Order Hold (ZOH).
(or the Sampling process)

Phase Detector Sampling Induced Delay

Fb/500 Phase Lag				
Run Length (UI)	Transition Density (ratio)	Sampling Period (sec)	Phase Lag at CL -3 dB (deg)	Phase Lag at est GH=1 (deg)
1	1.00	3.33E-10	0.36	0.23
2	0.50	6.67E-10	0.72	0.47
3	0.33	1.00E-09	1.08	0.70
4	0.25	1.33E-09	1.44	0.93
5	0.20	1.67E-09	1.79	1.17

Fb/10 Phase Lag				
Run Length (UI)	Transition Density (ratio)	Sampling Period (sec)	Phase Lag at CL -3 dB (deg)	Phase Lag at est GH=1 (deg)
1	1.00	3.33E-10	17.94	11.66
2	0.50	6.67E-10	35.89	23.33
3	0.33	1.00E-09	53.83	34.99
4	0.25	1.33E-09	71.78	46.66
5	0.20	1.67E-09	89.72	58.32

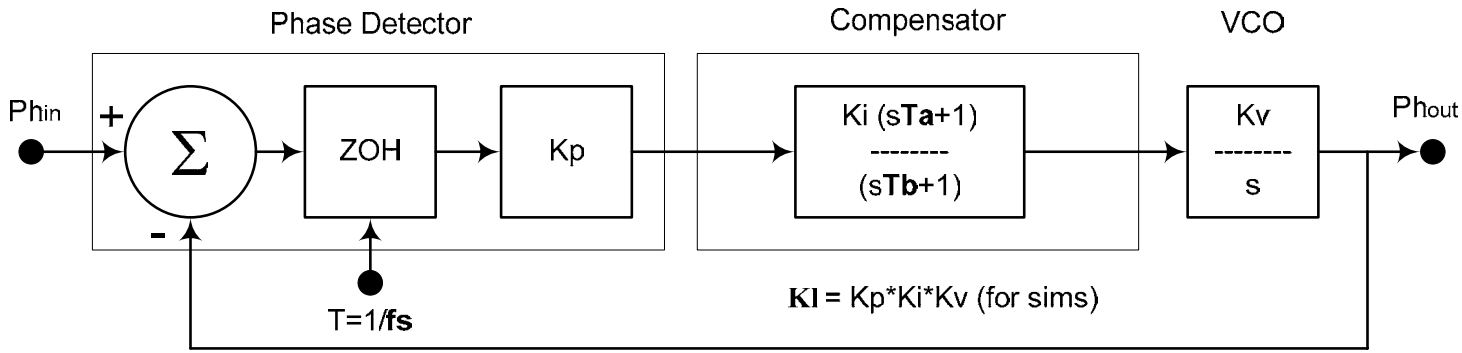
The point here is that PLL BW must be much lower than the lowest edge rate for good performance.

One effect of the phase detector sampling process is a time delay in the loop. This decreases the phase margin at the GH=1 (crossover) frequency. This reduces the jitter performance of the clock recovery system and reduces stability in the loop. Neither are desirable for a clock recovery system for jitter measurements. This phase lag can be approximated by wT/2 (in rad), where T (in sec) is the sampling period, and w (rad/s) is the frequency of interest.

The phase lag is shown at the -3dB corner frequency of the CL, just for reference. The phase lag at the open loop unity gain (GH=1) frequency, determines the loop stability. This frequency is about 0.65 times the -3dB CL frequency for this system.

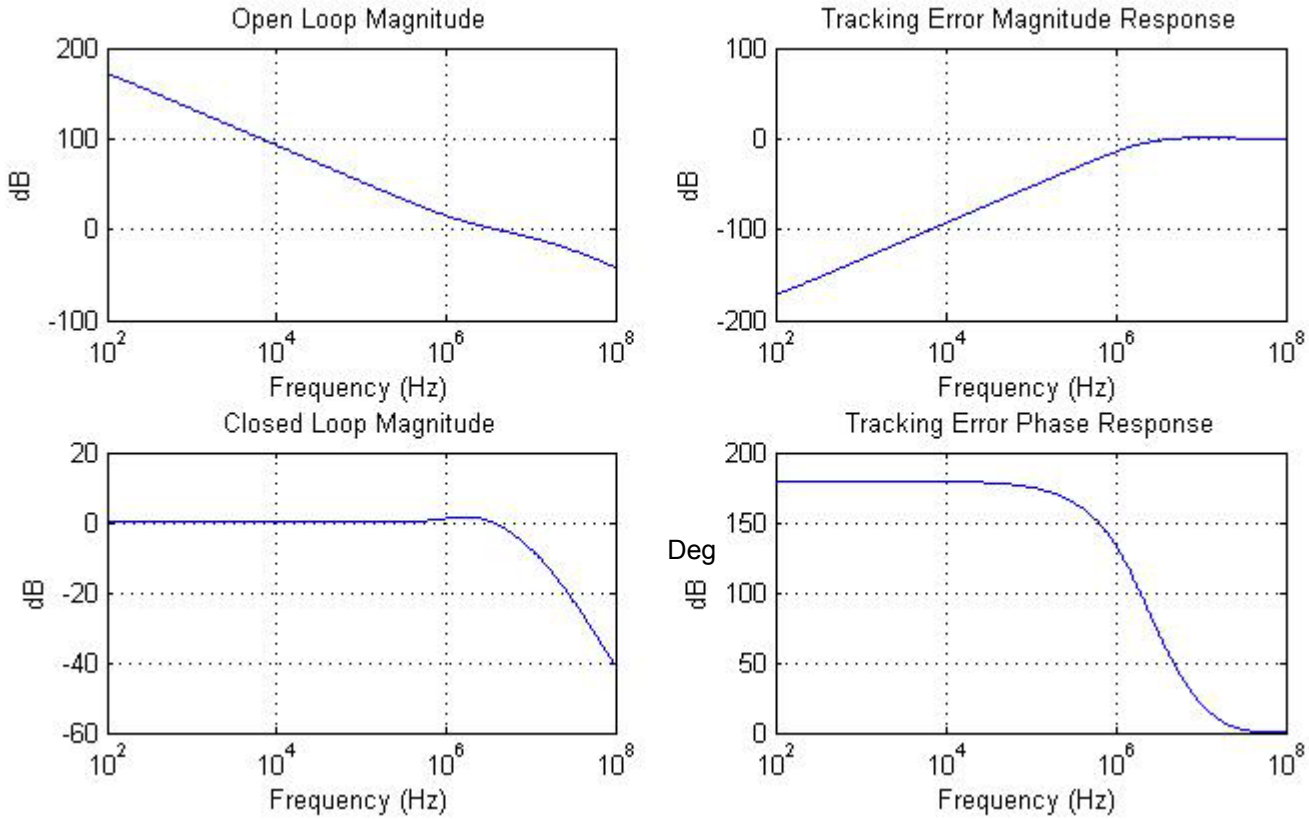
It can be seen that for Fb/500, the run length of the pattern has minor effects. For fb/10 the phase lag starts large and increases 5X over our allowable run length spans. (just due to time delay)

Example 2 Clock Recovery System



- This CR example is a Type I, second order PLL with a -20 dB/dec HF roll off.
- This alternate CR system compensation has been designed in order to compare the frequency domain characteristics to the previous Type II, third order PLL with a -40 dB/dec HF roll off.
- Note again, that the phase detector gain (Kp) has been held constant, as a function of RL (Run Length) to observe only the effects of the ZOH. In practice this will also vary, causing changes in open loop gain, closed loop BW and peaking.
- The compensator time constants have been set to produce a 300 Hz low pass filter (no integrator) and a zero that produces a lead at the same frequency as with the previous Type II design. The – 3 dB CLBW is also set to 6 MHz.
- For Reference, the resulting optimized parameters are provided:
  - Fb/500: Kl=1.15E11, Ta=1.43E-7, Tb=5.30E-4

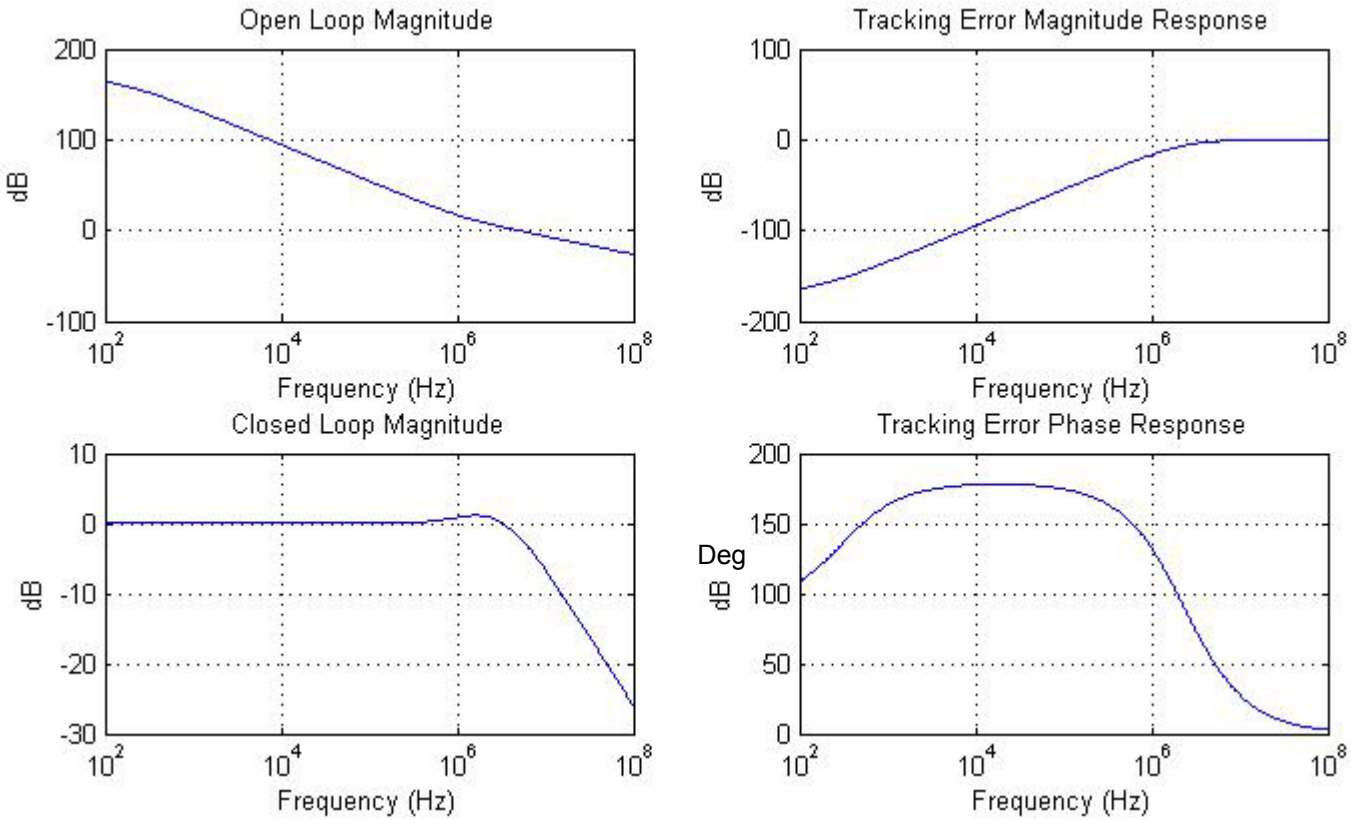
Example 1: TYPE 2, 3rd Order, PLL -40 dB/dec CL HF Roll Off



Tracking Error Magnitude HP Function is 40 dB/dec, as desired.

The Tracking Error is the JTF.

Example 2: TYPE 1, 2nd Order, PLL -20 dB/dec CL HF Roll Off



Tracking Error Magnitude HP Function is 40 dB/dec, as desired.

The Tracking error is the JTF.

A comparison of Tracking Error on PLLs of different “TYPE” classes.

- Two PLLs of different TYPEs and Orders are compared to show that, the same SSC frequency component suppression can be achieved in either case.
- Both PLLS were tuned for a 6 MHz -3dB CL loop gain point with a Dt = 1.0. (as per the present spec)
- The TYPE 2 PLL has a Integrator in the compensation, the TYPE 1 PLL has a 300 Hz LPF in the compensator **but no integrator**.
- The graph at the upper right is the Tracking Error Magnitude, which is the basis of our jitter definition. (High Pass Function shaped JTF)
- Also compare the peaking in the Closed Loop magnitude response to the peaking in the Tracking Error Magnitude. Allowing peaking in the closed loop response, does not infer peaking in the Tracking Error or JTF Magnitude.

SSC Frequency Component Tracking

The following numerical data is extracted from the simulation runs of the two PLL types shown on the previous pages. It can be seen that equal SSC tracking capability can be achieved with either “type” PLL structure. What is important is the open loop gain at the SSC frequencies.

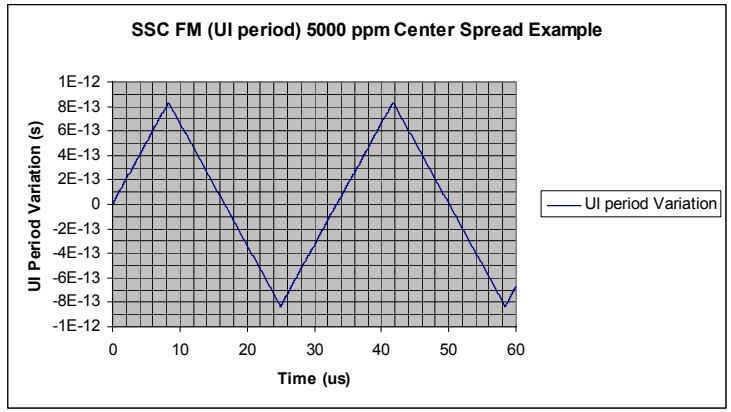
PLL Tracking Error (SSC Suppression) Comparison					
SSC Harmonic #	SSC Freq (KHz)	Type 2 Mag (dB)	Type 2 Phase (deg)	Type 1 Mag (dB)	Type 1 Phase (deg)
1	30	-73.7	178.5	-75.6	177.9
3	90	-54.8	175.6	-56.6	175.2
5	150	-45.8	172.6	-47.6	172.1
7	210	-40.1	169.7	-41.9	169.1

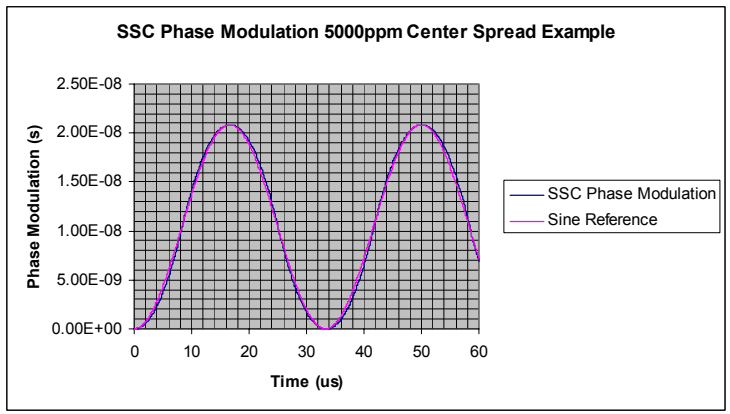
The Type 1 actually shows slightly lower (better) tracking error. This is due to the fact that the two systems were tuned for a CLBW of 6 MHz, and the shape of the closed loop response of the two systems is different in that region.

The point is, that requiring a “Type 2” loop is actually over constraining the requirements of the PLL. The tracking capability, at the SSC frequencies, is what is important. There is a better way to define this desired tracking behavior. (the JTF) A pure Type 1 loop would not have sufficient SSC tracking capability. This comparison is intended to highlight the fact that a Jitter Definition based on the JTF controls the desired characteristics independent of nomenclature. The requirements are clearly defined by the JTF.

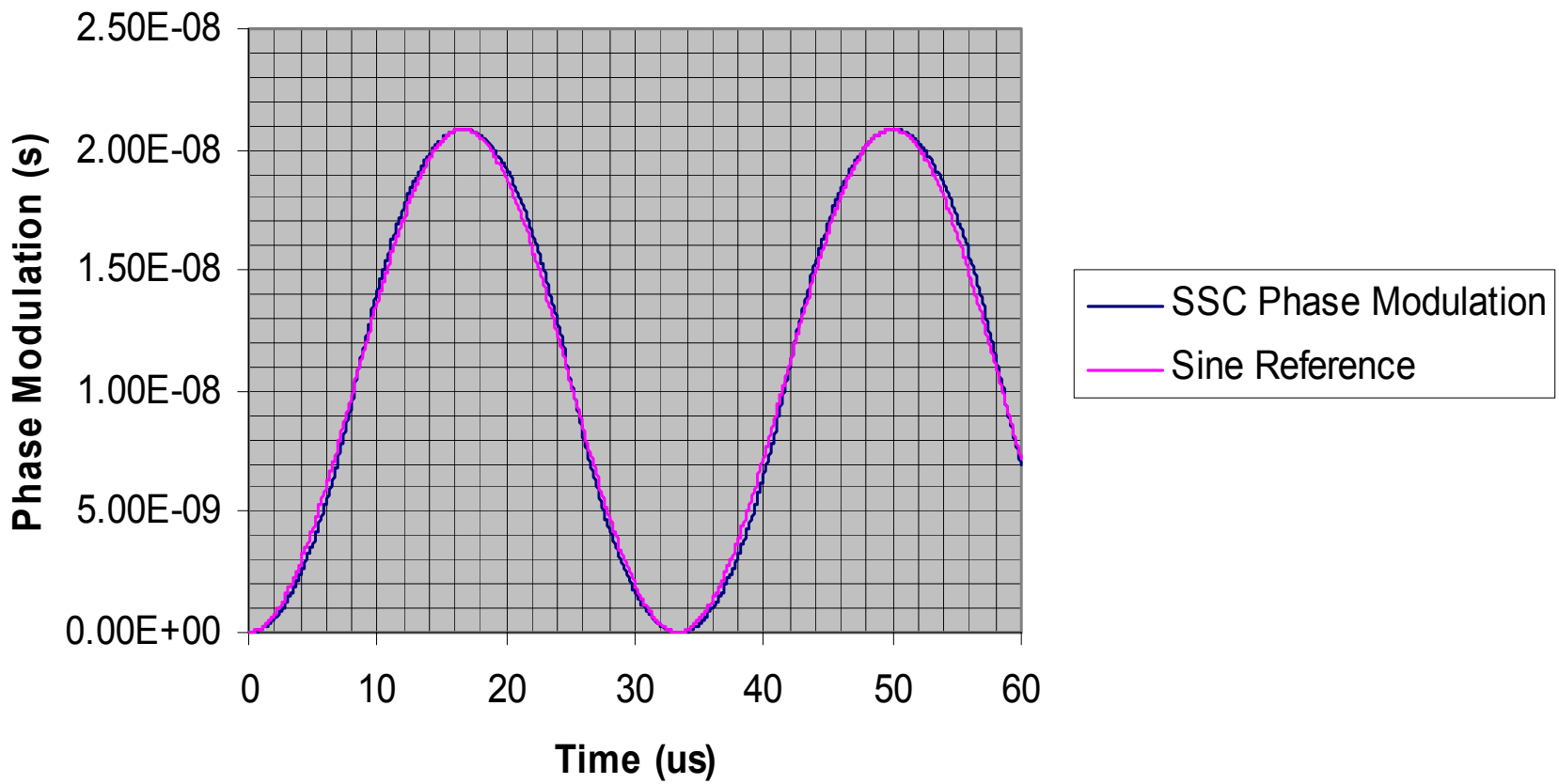
SSC Comments

- PLL transfer functions are based on Phase Modulation (PM) rather than Frequency Modulation (FM). Phase variation is the integral of Frequency variation. Triangular FM SSC, integrates into a sine-like PM. (actually it is a parabola – but close to a sine)
- The top simulation plot shows the period (1/freq) variation of a Gen2 UI for 5000 ppm, 30 KHz SSC. (center spread was used to simplify the simulation initial conditions) 1.667ps p-p
- The bottom simulation plot shows the integral of the triangular FM, or the PM (in blue). The magenta curve is an ideal cosine curve plotted with the same scaling and offset for comparison. (both are 20.83 ns p-p)
- For triangular SSC, the integration can be easily done graphically on paper, and the p-p value matches the simulations. (profiles other than sine and triangular, require computer assistance)
- This shows the rational for using a 20.83 ns p-p sine wave at 30 KHz for an approximation of the triangular SSC FM. (The integral of a Sine Wave is a scaled Cosine - inverted) This is not the exact SSC PM, but it is close enough for measuring attenuation at 30 KHz and some quick SSC leakage checks.





Expanded SSC PM View (from the last Slide)



Better View?

Section 2 Key points

- Specifying only the closed loop characteristics of a PLL does not sufficiently control the tracking error characteristics of the PLL. Including PLL nomenclature and additional terms such a damping, still allows for varying results.
- The ratio of PLL Phase Tracking Error to sinusoidal Input Phase Modulation, as a function of frequency, is the JTF or Jitter Transfer Function.
- The JTF is direct method of describing what jitter the receiver will see if the receiver has the same characteristics as the referenced PLL characteristics. This also defines how JMDs should measure this jitter.
- In the frequency range of interest, the same JTF may be achieved by multiple design implementations. This JTF Jitter Definition also allows for all several classes of JMDs to be valid for compliance measurement.
- PLL Characteristics are based on Phase (or time) modulation, not Frequency modulation. Phase modulation is the integral of Frequency modulation. SSC is typically specified in frequency modulation terms.

Section 3

Shifting to a New Jitter Definition

Why do we need to Change?

- The present definition specifies Bandwidth in the Closed Loop Transfer Function (CLTF) and a damping factor, as an attempt to control the Jitter Transfer Function (JTF) of the PLL that defines our Reference Clock. The Reference Clock tracking ability defines the separation of Jitter from SSC and low frequency trackable jitter.
- It has been shown that:
  - The BW of the JTF is different that the BW of the CLTF
  - The Peaking of the CLTF is different than the Peaking of the CLTF.
  - Specifying the “zeta” in a Type 2 loop, or eqv. (trying to prevent peaking) is not valid.
  - Specifying or measuring CLTF characteristics, provides no way to insure that the JTF of the Reference Clock PLL has a unique and defined set of characteristics.
  - The present Jitter Definition allows for multiple interpretations, that prevent multiple Jitter Measuring Device (JMD) types from converging on similar results, even on simple Jitter test signals.
- By not having a clear definition of what is considered jitter and what is considered to be allowable timing variations, interoperability may be endangered.
- A unified means of verifying the JTF of JMDs, is required to minimize the observed differences in measurement results that may degrade interoperability margins. A means of validating TJ approximation methods (that save valuable test time) must be preserved. The JTF of these JMDs used for TJ validation (Full Population BERT Scan) must be verified as well, to improve correlation between units.

A Quote: The Significant problems we face cannot be solved at the same level of thinking we were at when we created them. – Albert Einstein

The Plan

The intent of the New Jitter Definition in this example (SATA Gen2i), is to preserve the present jitter requirements for the TX and RX jitter tolerance as defined in the present definition, as if the present definition was interpreted properly. (as much as possible) In some cases, maintaining interoperability supersedes preserving previous issues caused by the misinterpretation. This may result in some possible differences in reported jitter performance of present devices.

Jitter Definition Goals

- Provide a clear definition of what is jitter and what is considered SSC or low frequency track able variations.
- To emulate the characteristics of what could be considered an acceptable CDR that could be used in a system and achieve the required BER. (a reference design)
- Allow for the verification of the measurement accuracy of JMDs (Jitter Measuring Devices).
- Allow for a wide range of commercially available JMD classes to be used for jitter measurements. Each have their advantages.
- Provide for an actual measurement standard, used to qualify the TJ measurements provided by various TJ approximation methods.

What to do for an improved Jitter Definition?

(General Details of the Definition)

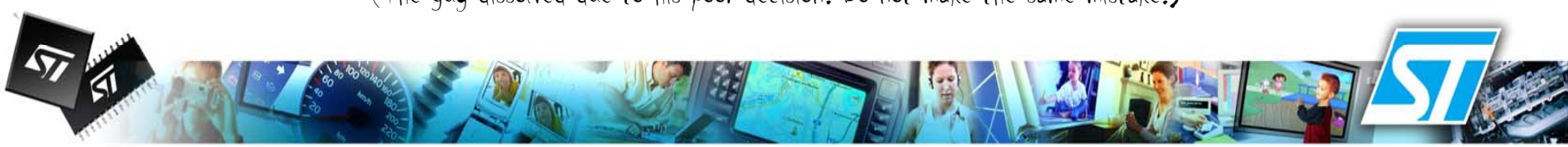
- Specify sinusoidal PJ tracking error as a function of frequency (JTF) as the normative requirement. (include allowable tolerance) This would be done for a D24.3 pattern. (Dt = 0.5)
- In the normative requirement, specify the JTF down to the fundamental frequency of the SSC with a level of Sinusoidal Jitter at 30 KHz equivalent to the maximum allowable SSC specified.

  (but as Phase or Time Modulation)
- Closed Loop PLL characteristics could be provided as informative data to approximate the necessary CR in some JMDs. (Since CL characteristics are the typical specifications provided for CR based systems.) Other informative data could include the advice that a Type II PLL or one with equivalent tracking capability at 30 KHz and above is necessary to meet the normative requirements.
- Define the measurement conditions required to verify the characteristics of the JMD used to measure TX jitter and qualify the applied jitter for RX Jitter Tolerance.

Trade Offs and Considerations

- Tightly specifying a JTF, will promote better correlation between JMDs and receivers and between multiple JMDs.
- Being too tight on the JTF specifications may eliminate some useful JMDs.
- JMDs containing PLLs usually specify the CL characteristics. The JTF can easily be measured (on any JMD), but it is not usually provided at this time in our industry as a specification. This may change with the JTF acceptance.
- Since the JTF is the controlling parameter, actual settings on JMDs are secondary to the required response. A one time calibration and verification of the JTF provides the suggested JMD settings required to achieve the desired response. (In your Lab and/or at the JMD manufacturers Lab.)

A Quote: He chose poorly! –From an Indiana Jones Movie
(The guy dissolved due to his poor decision. Do not make the same mistake.)



Now, with that in mind, lets consider the required elements of the New Jitter Definition.

New Jitter Definition Key Elements

- The new Jitter Definition will define the JTF BW that would be equivalent to the present Jitter Definition CL BW of fb/500 or 6 MHz for Gen2i. Since this is not a unique transformation, a “typical” translation of BW will be determined. This will be the Normative requirement. An Informative, typical, CL BW will be maintained (6 MHz) to aid with the set up or selection process.
- The peaking in the JTF must make allowances for the required ability to track SSC. This tracking ability requires a Type 2 loop or a Type 1 loop with the same loop gain and phase characteristics down to 30 KHz. (and therefore the same peaking) To eliminate most of the peaking in the JTF, a pure Type 1 loop would be required. This would not allow for enough loop gain at the SSC frequencies (fundamental and harmonics) to remove most of the SSC effects in the jitter measurements. Typical Type 2 JTF peaking will be used to determine the nominal value.
- The JTF attenuation at the SSC fundamental frequency will be defined. Besides insuring a Type 2 or equivalent Loop Gain for SSC tracking, it constrains the low frequency end of the JTF, while the BW and peaking constrains the higher frequency end of the JTF. The BW is affected by peaking, but the attenuation at the SSC fundamental is more definitive.
- The JTF characteristics will be specified for a pattern with a transition density of 0.5. This is close to typical random 8b10b encoded data transmission. Changes of BW and peaking, as a function of transition density, vary widely with JMD types. All jitter test patterns should have a 0.5 transition density for the best correlation between JMDs. (unless JMD post processing methods emulate PLL characteristics changes with Dt.)
- As previously stated, tighter definitions allow for better correlation between measurements, but if the definition is too tight, some JMD classes of equipment may be eliminated. (we need to avoid this)
- The JTF of the JMD must be able to be verified, without vendor specific means.

Equivalent JTF Bandwidth

In order to determine the equivalent JTF BW, to that of the present CLTF BW of fb/500 (6 MHz for Gen2i) a series of measurements and simulations on Type 2 (or equivalent G(s) functions above 30 KHz) were collected. The goal here is to determine the typical value and range of the ratio JTF BW / CLTF BW. It has been shown that this is not a unique ratio, so a sample of practical devices is necessary to translate this present BW specification.

Type 2* Measured and Simulated Data

The data below, was collected from hardware clock recovery systems and from simulations of practical clock recover systems. All were Type 2 or equivalent*. A pure Type 1 is not valid since it does not provide the required SSC frequency component rejection. In all cases the transition density (Dt) of the pattern matched the expected Dt setting of the CR system. (only test equipment data and simulations are present in the list) The list is sorted by increasing JTF attenuation at the SSC fundamental frequency of 30 kHz.

CLTF BW (MHz)	CLTF Peaking (dB)	JTF BW (MHz)	JTF Peaking (dB)	JTF 30 KHz Attn (dB)	BW Ratio JTF/CLTF (#)
6.9	1.08	2.2	4.09	67.2	0.32
9.2	0.99	2.3	4.30	67.9	0.25
6.5	0.91	2.8	1.84	68.6	0.43
6.5	0.92	2.9	1.64	70.6	0.45
8.8	2.13	2.0	4.30	73.7	0.23
6.8	2.22	1.9	3.66	73.7	0.28
6.3	1.60	2.8	1.23	73.9	0.45
6.5	2.05	2.4	2.05	75.3	0.37
6.5	2.04	2.4	1.92	77.4	0.37
Average			2.78	72.03	0.35
Min			1.23	67.20	0.23
Max			4.30	77.40	0.45

The BW Ratio of the JTF to the CLTF (last column) on average is 0.35x. In this sample, it ranges from 0.23x to 0.45x. For the present CLTF BW of 6 MHz, the average equates to a JTF BW of 2.1 MHz.

If the JTF BW was defined to be 2.1 MHz, then the observable range of CLTF BW (an available setting) would vary from 4.7 MHz to 9.1 MHz for this sample. The DT=0.5 post processing HPF setting would be 2.1 MHz.

Looking at our present Jitter Definition, a CLTF BW specification of 6 MHz, results is a JTF BW of 1.4 MHz to 2.7 MHz for this sample. By specifying the JTF, a 2:1 variation in BW is removed. At a 40 dB/dec slope of the JTF, this equates to a 12dB change of jitter levels at frequencies below the corner frequency at present.

* = Type 1 loops with the same G(s) as a Type 2 loop, at frequencies above 30 KHz are also valid.

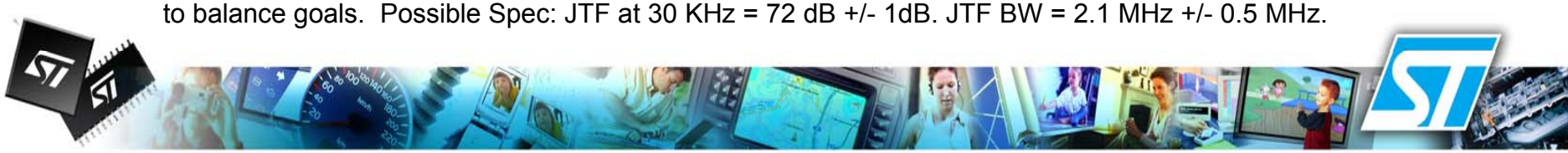
Additional Jitter Definition Parameters

CLTF BW (MHz)	CLTF Peaking (dB)	JTF BW (MHz)	JTF Peaking (dB)	JTF 30 KHz Attn (dB)	BW Ratio JTF/CLTF (#)
6.9	1.08	2.2	4.09	67.2	0.32
9.2	0.99	2.3	4.30	67.9	0.25
6.5	0.91	2.8	1.84	68.6	0.43
6.5	0.92	2.9	1.64	70.6	0.45
8.8	2.13	2.0	4.30	73.7	0.23
6.8	2.22	1.9	3.66	73.7	0.28
6.3	1.60	2.8	1.23	73.9	0.45
6.5	2.05	2.4	2.05	75.3	0.37
6.5	2.04	2.4	1.92	77.4	0.37
Average			2.78	72.03	0.35
Min			1.23	67.20	0.23
Max			4.30	77.40	0.45

First an observation: The general trend shows that additional attenuation at 30 KHz, results in additional peaking in the CLTF. Our present definition attempt to eliminate peaking in the CLTF, resulting in requiring a pure Type 1 loop which would not provide the necessary SSC suppression. Some peaking must be allowed.

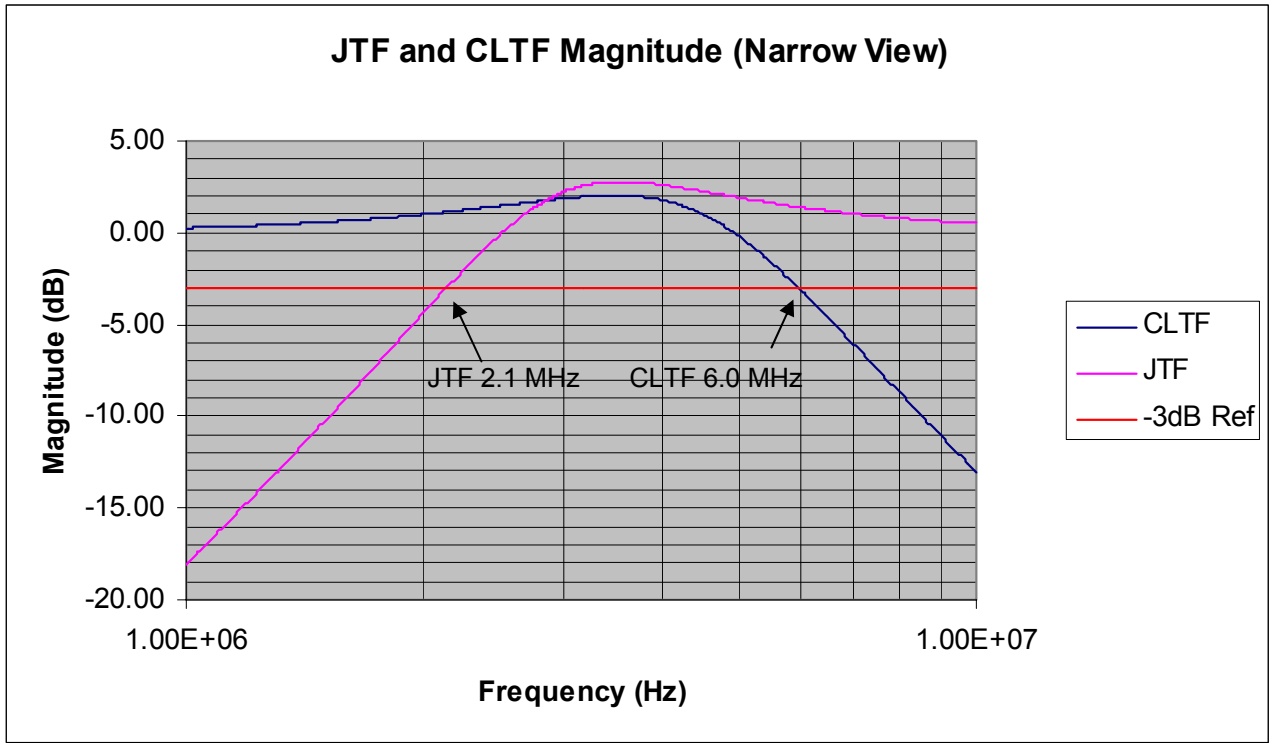
In the case of the JTF peaking, the average is 2.8 dB, and can range from 1.2 dB to 4.3 dB. A distinct trend is not observed, due to the allowable variations in G(s) in particular designs. A spec of 2.75 dB +/- 1.5 dB could be used. This would result in variation of jitter measured jitter levels in the peaking region, (3dB range) but controlling the attenuation between the BW frequency and 30 KHz provides an improvement over about 2 decades of frequencies. (12 dB variation at present)

If the integral of the 5000ppm triangle SSC **Frequency** modulation at 30 KHz, is approximated by a **Phase** modulation of a 62.5 UI (20.83 ns) p-p sine wave at 30 KHz (it is actually more parabolic) the average JTF attenuation at 30 KHz of 72 dB results in an increase of DJ of 5.2 ps when SSC is active. Over the range of attenuation, in this sample, the SSC “Leakage” expected would be 2.8 ps to 9.3 ps p-p. (3 to 11 ps has been observed with actual Lab Source SSC tests) A 30 KHz JTF spec level could be 72 dB +/- 5 dB. (Using the 6 cases with the JTF BW closest to 2.1 MHz the nominal is 72.5 dB.) This parameter defines the positioning of the 40 dB/dec slope. The tolerance of this should be reduced, and the BW tolerance relaxed, to balance goals. Possible Spec: JTF at 30 KHz = 72 dB +/- 1dB. JTF BW = 2.1 MHz +/- 0.5 MHz.



A Graphical Look at the JTF and CLTF (1)

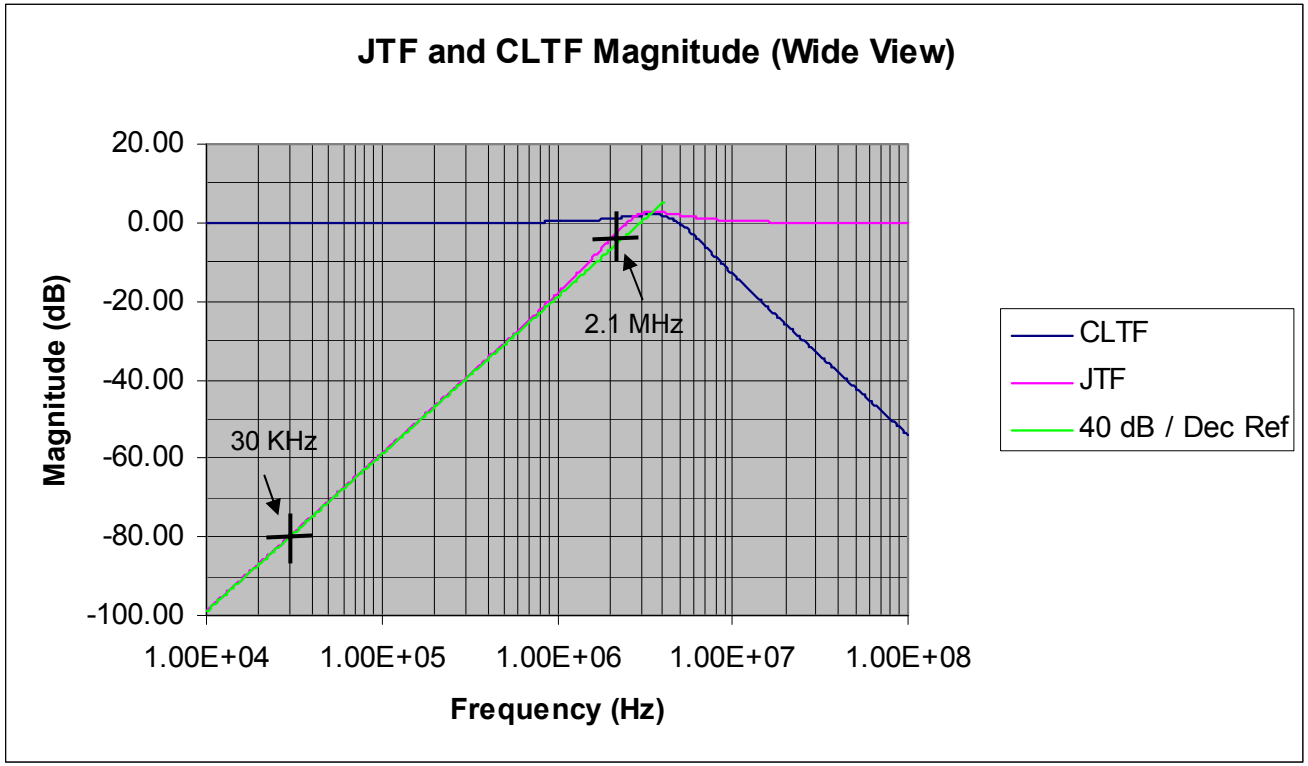
This plot shows a JTF BW of 2.1 MHz. and JTF peaking of 2.75 dB (The nominal JTF definition.) The corresponding nominal CLTF BW is 6.0 MHz, with a peaking of 2.0 dB. (Present Jitter Definition BW with peaking.)



In the narrow frequency range view, the difference in the -3dB BW of the two functions is apparent. One can also see the amount of reported jitter increase that would be present in the 2.5 MHz to 7 MHz region caused by the required JTF peaking.

A Graphical Look at the JTF and CLTF (2)

This plot shows a JTF BW of 2.1 MHz. and JTF peaking of 2.75 dB (The nominal JTF definition.) The corresponding nominal CLTF BW is 6.0 MHz, with a peaking of 2.0 dB. (Present Jitter Definition BW with peaking.)

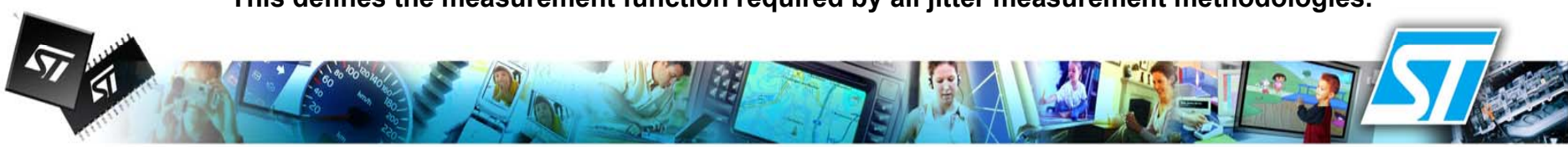


In the wide frequency range view, it can be seen that if the JTF attenuation at 30 KHz is specified and the JTF -3dB BW is specified, the resulting attenuation over 2 decades is controlled. (For a Type 2 PLL or equivalent.) Some deviation from the ideal slope is observed near the JTF corner frequency. This depends on the G(s) and the resulting peaking. (A tighter spec at 30 KHz and more tolerance at -3dB allows for variation in designs, and yet preserves the characteristics for most frequencies.)

SATA Gen2i New Jitter Definition Proposal

(Rev B: Tolerances have been adjusted to allow for practical measurements)

- Jitter is the short-term variations of the zero crossings from ideal positions in time. A "Reference Clock" (defined in section 7.3.2) defines the ideal positions in time. *(Sec 7.3, p 185)*
- The Reference Clock definition (Sec 7.3.2, p 186) states:
  - Reference clock extraction is performed using either hardware or software PLLs.
  - The PLL is Type 2 (Or has the same JTF as a Type 2 PLL for all frequencies equal to or greater than 30 KHz.)
  - The JTF attenuation of 20.8 ns p-p +/- 10% Sinusoidal Jitter at 30 KHz +/- 1% shall be 72 dB +/- 3 dB.
  - The JTF -3dB BW shall be 2.1 MHz +/- 1.0 MHz. The JTF peaking shall be 3.5 dB Max. (using 0.3 UI p-p +/- 10% sinusoidal PJ)
  - The JTF of the PLL is defined for a pattern with a transition density of 0.5. (a D24.3 pattern 11001100… shall be used for JTF verification)
  - Informative: A type 2 PLL (or equivalent for frequencies equal or greater than 30 KHz) with a CLTF -3dB BW of fb/500 or 6 MHz and 2.0 dB peaking may provide characteristics close to the required JTF. Adjustment of the CLTF settings must be made to match the JTF requirements, due to variations of PLL characteristics, from unit to unit. A CLBW setting of 4 MHz to 10 MHz could be necessary to achieve the JTF requirements.
  - Informative: Phase characteristics of post processing filters or simulated PLLs used in some JMDs, must match the phase characteristics of the defined PLL JTF, to maximize correlation between JMDs, for typical mixed Jitter component compositions. Minimal phase implementations assist in meeting this goal. The JTF phase is not typically observable on all classes of JMDs, so this can not be made a Normative requirement. If discrepancies are seen, the JMD with the closest phase characteristics to the defined PLL shall be considered as having the proper JTF.
- Jitter Measurements (Section 7.4.7, p 214) further states:
  - The BERT scan method described in section 7.4.7.1 is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. (Direct measurement to a BER 1E-12)
  - The clock recovery circuit has the defined low pass function H_L. The time difference between the reference clock and the data, results in a high pass function H_H. The resulting jitter seen by the receiver has the high pass function H_H. This high pass function is the Jitter Transfer Function (JTF). **This defines the measurement function required by all jitter measurement methodologies.**



Rev B Jitter Definition

- The Rev B of the proposed jitter definition has tolerances adjusted and one added for the 30 KHz test signal, to be complete. Practical Lab measurements have shown that this would improve the JTF verification process.
  - The JTF Attenuation tolerance has been widened to 72 +/- 3dB from +/- 1 dB since even with the wider range, the measured allowable values for a 20.83 ns p-p sine test signal range from 3.7 ps to 7.4 ps of DJ increase when the test signal is applied. Even with this range, it may be necessary to take multiple measurements and record the mean, depending on the stability of the source and the JMD. (a small jitter value)
  - The tolerance of the -3dB BW has been widened to 2.1 MHz +/- 1 MHz due to the large effect of peaking on the -3 dB frequency. The historical -3dB point is close enough to the peaking region, that there is a strong effect of peaking on this value, even when the JTF slope is the same at lower attenuation levels and frequencies.
  - The test signal for measuring the attenuation at 30 KHz needs to have a tolerance added to be complete. Since the measurement is a ratio of the resulting DJ increase to the test signal DJ, the absolute value is not critical, but has been chosen to reflect typical phase modulation produced by the maximum SSC level allowed in the SATA spec. The test signal amplitude is now defined as 20.8 ns +/- 10%.
  - The peaking is now controlled by a Maximum level of 3.5 dB. (1.5X) The initial value forced a minimum peaking value. Simulated PLL JMDs can match the other criteria without introducing peaking. Hardware CR units, due to the phase lag caused by a sampled phase detector need to be allowed to have some peaking in the JTF. (The SW simulated PLLs did not include this limitation.) Since the ideal JTF would have no peaking, and we would like to encourage minimal peaking in HW CR units, the maximum level was placed at realistic limit but at a level that is bit of a challenge for some configurations. Reporting 150% of that actual value is the maximum we should allow.

Comments on New Jitter Definition

- The JTF is defined with a Dt=0.5. This is a departure from the present spec that defines the CLTF BW with a Dt=1.0 and then expects a reduction of BW to approximately 50% when testing with typical 8b10b encoded data with a Dt = 0.5. This has been changed for the following reasons:
  - The present CLTF BW of 6 MHz typically results in a JTF BW of 2.1 MHz. If the BW set at Dt=1.0 and used at Dt=0.5, there is AT LEAST a 2:1 reduction of JTF BW to about 1 MHz. The amount of SSC component attenuation at 30 KHz would be only about 60 dB on average. (assuming that at 2.1 MHz 72 dB is typical) This adds about 21ps of measured TX DJ, when SSC is active, for quality SSC modulation.
  - At present, some post processing methods have erroneously assumed the JTF BW (the high pass function) has the same BW as the CLTF. (6 MHz) Correcting this misconception, resulting in a 3X reduction in BW, is less of a shift that keeping the Dt=1.0 calibration setting and forcing a 6X reduction in BW.
- This Jitter Definition has been focused on SATA Gen2i and it applies to Gen2m. Gen2x at present, has a basic problem (besides using values from SAS and test methods from SATA). The Fb/1667 or 1.8 MHz CLTF BW, results in a typical JTF BW of 630 KHz. Even with the change of the calibration Dt to 0.5, the resulting TX DJ increase when SSC is active, could be 58 ps p-p (33ps to 70ps has been observed in simple checks.) The value is a function of G(s) and CLTF peaking. If the Dt=1.0 BW calibration is used, this could reach 234 ps p-p! (JTF BW = 315 KHz) Fb/1667 is the present Gen2x spec., and no refinement of the Jitter Definition will help Gen2x track SSC sufficiently.

Section 3 Key points

- There is a need to change to a more clear Jitter Definition method in order to improve correlation between jitter measurements while matching the jitter that the reference actually receiver “sees”. This improved correlation results in improved interoperability. This becomes more important as jitter budgets become tighter at higher data rates.
- In this example, a JTF definition was generated by the typical or average JTFs, achieved by multiple CR units set to the previous CLTF based Jitter Definition. This was done to preserve the original intent of the jitter definition. For a new standard, a theoretical basis, tempered with practical constraints, could be used.
- It is important to consider how the JTF requirements are to be verified when defining the test levels and tolerances in which the JTF characteristics must be achieved. The JTF test levels should represent the typical operating points of the CR unit in normal operation, or be within the compliance test level ranges.

Section 4

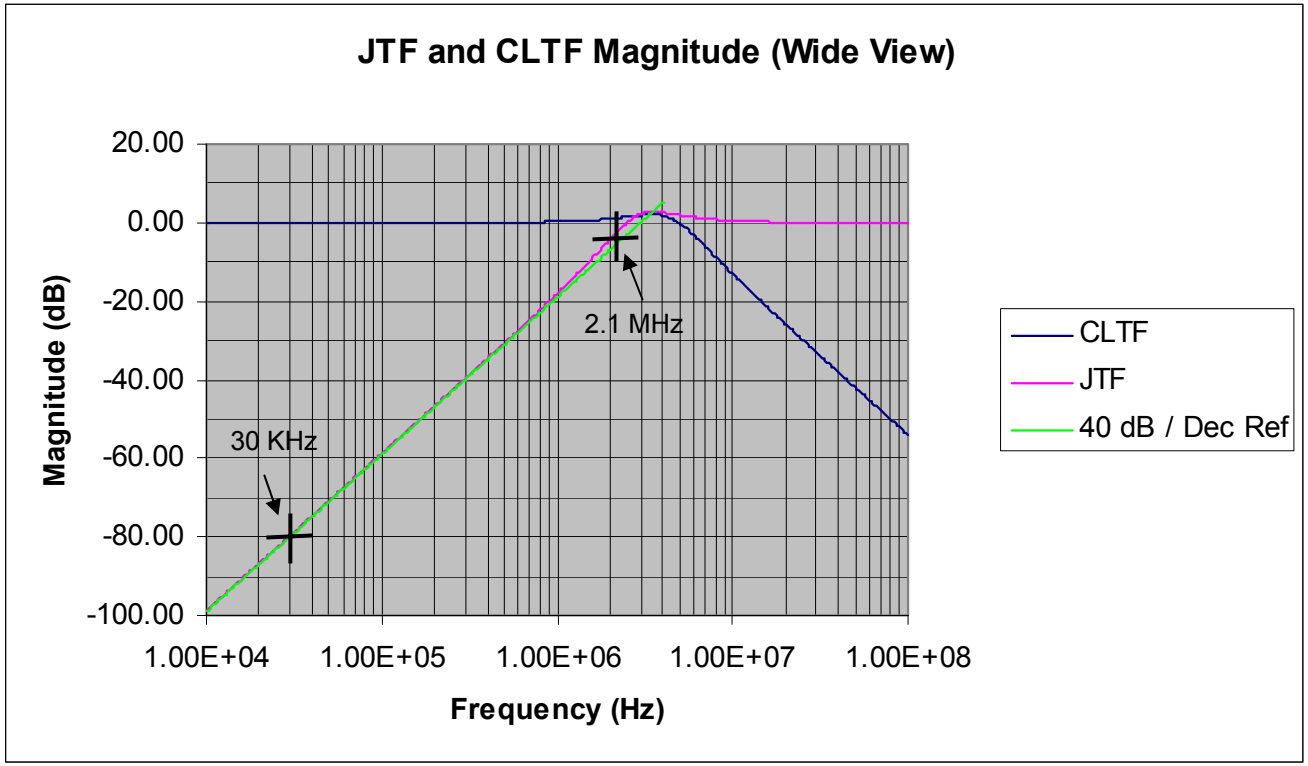
JTF Verification Method

Gen 2i JTF Verification

- When measuring the JTF magnitude, the concept is simple: Apply a clean sinusoidal PJ source with a known level and verify the JMD reports the correct level of jitter. This allows for a wide range of JMDs that may be used to measure to our jitter definition. (including post processing with fixed BW filters, if the Dt of test patterns is held at 0.5)
- 1) The Test signal for measuring the JTF attenuation at 30 KHz +/- 1% contains 20.8 ns p-p +/- 10% Sinusoidal Jitter. (adjust the CLTF BW with nominal peaking to achieve the attenuation requirement.)
- 2) The Test Signal for measuring the JTF BW and peaking contains 100 ps p-p (Gen2 = 0.3 UI p-p) sinusoidal Jitter, with no RJ added. (modifications to the CLTF BW and peaking settings, may be required to achieve both the attenuation at 30 KHz, and the -3dB BW of the JTF)
- A clock like data pattern is used, (no ISI) with a Dt = 0.5 (this is where we operate and where CR units are specified) A D24.3 is the test pattern. (11001100…)
- Other Information:
  - TX Jitter and RX Jitter Test Patterns in our specification ideally should also have a Dt = 0.5 for the best correlation. Using patterns with Dt different from the calibration point is possible but added variation will be observed depending on how the JMD JTF BW varies with Dt.
  - With a relatively pure Sinusoidal PJ source, a lot of alternative methods are available to validate the level of the PJ Test source. (Most JMDs can do this if the test signal is not contaminated with other jitter components.)

A Graphical Look at the JTF (History - for Reference)

This plot shows a JTF BW of 2.1 MHz. and JTF peaking of 2.75 dB (The nominal JTF definition.) The corresponding nominal CLTF BW is 6.0 MHz, with a peaking of 2.0 dB. (Present Jitter Definition BW with peaking.)



For setting or verifying the characteristics of the JMD, the goal is to match the attenuation-frequency at the two points shown on this plot. (within specified tolerances) Since phase is not observable in many JMDs, only the magnitude is a normative requirements at this time. Limiting the peaking of the JTF is also required.

Practical JTF Measurements Suggestions

- Either the attenuation at 30 KHz or the -3dB BW may be measured first. Adjustments of JMD settings (CL BW or HPF BW) and peaking if available, are performed to balance the two criteria. When the all criteria are met, the JMD is tuned to the New Jitter Definition.

- Here is a step by step example of a JFT measurement. (others exist)
  1. Adjust the pattern generator and modulation to produce a 30 KHz, 20.8 ns p-p nominal sinusoidal modulation. (Gen2 D24.3 Pattern)
  2. Verify the level of modulation meets the requirements and record the p-p level (DJ_t). This can be done with Time Interval Error (TIE) type measurement or equivalent.
  3. Apply this test signal to the JMD. Measure the **difference** in DJ reported when the modulation is on, minus the level when it is off. (DJ_m)
  4. Calculate the Attenuation: 20Log(DJ_m / DJ_t) Adjust the JMD settings to match the attenuation requirements at 30 KHz.
  5. Apply 0.3 UI p-p +/-10% sinusoidal PJ at a frequency much greater that the expected BW (100 MHz has been used, but any frequency in "flat region of the JTF may be used) This is the "0dB" reference. The absolute value of the PJ level does not need to be precise, but it should be verified that the level remains constant between the 0dB reference point and the BW frequency. Record the JMD reported DJ level when the PJ is applied, **minus** the reported DJ when the PJ is off. (DJ_{0dB})
  6. Calculate the -3dB value: $DJ_{-3dB} = DJ_{0dB} * 0.708$
  7. Shift the frequency of the PJ source until the reported DJ **difference** between PJ on versus PJ off is equal to (DJ_{-3dB}) The PJ frequency is the -3dB BW of the JTF.
  8. Check the peaking of the JTF. Starting at the BW frequency increase the PJ frequency until the maximum reported DJ frequency is located. Then measure the reported DJ level when the PJ is on, **minus** the reported DJ level when the PJ is off. (DJ_{pkng})
  9. Calculate the JTF Peaking value: 20Log (DJ_{pkng} / DJ_{0dB})
  10. Make adjustments to the JMD to balance the JTF requirements as needed. These are now the proper JMD settings to make Gen2i Jitter measurements.

This only needs to be done once or during calibration checks. (Unless you are bored, then it can be done weekly.)

Section 5

An Improved Jitter Definition Specification Example

Final Example Specification (1)

7.3.2.1 Gen2i and Gen2m Normative Requirements

For Gen2i and Gen2m, the Reference Clock characteristics are controlled by the resulting JTF (Jitter Transfer Function) characteristics obtained by taking the time difference between the Type 2 PLL output (the Reference Clock) and the data stream sourced to the PLL. The PLL CLTF -3 dB corner frequency, and other adjustable CLTF parameters such a peaking, are determined by the value required to meet the requirements of the JTF. (See section 7.4.7 for JTF information)

The JTF for Gen2i and Gen2m shall have the following characteristics for an encoded D24.3 pattern (1100110011 0011001100). This is the MFTP which is a test pattern that has clock-like characteristics and a transition density of 0.5.

1) The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
2) The magnitude peaking of the JTF shall be 3.5 dB maximum.
3) The attenuation at 30 KHz +/- 1% shall be 72 dB +/- 3 dB.

The JTF -3dB corner frequency and the magnitude peaking requirements shall be measured with sinusoidal PJ applied, with a peak-to-peak amplitude of 0.3 UI +/- 10%. The attenuation at 30 KHz shall be measured with sinusoidal phase (time) modulation applied, with a peak-to-peak amplitude of 20.8 ns +/- 10%.

Final Example Specification (2)

7.3.2.2 Gen2i and Gen2m Informative Comments

Typically a CLTF -3 dB corner frequency of fBAUD /500 could provide a JTF with characteristics close to the requirements, but due to differences in Type 2 PLL designs, the actual CLTF settings required to meet the required JTF can vary widely.

It is desired that the phase response of the JTF of a JMD (Reported Jitter / Applied Jitter) be that of the JTF of the time difference of the output of a Type 2 PLL to the Data stream applied to the PLL. This is the reference design. In the presence of multiple jitter component frequencies, the relative phase at these frequencies determines how they are combined to construct the final reported jitter value. In the case of discrepancies between the reported jitter levels, between JMDs with the same JFT magnitude response, the JMD with the JTF phase characteristics closest to that of the reference design, is to be considered correct. The JTF phase response of a JMD is important, but it is not always possible to determine this without proprietary information concerning the JMD processing methods, and it is not externally observable in some classes of JMDs.

The JTF of the time difference of the output of a Type 2 PLL to the Data stream applied to the PLL, or the reference design, is defined with a pattern that has a transition density of 0.5. Since this Type 2 PLL contains a sampled data mode phase detector, with a gain that varies proportionally with transition density, the JTF -3 dB corner frequency will change with the transition density of the applied pattern. For a well designed PLL, with significant phase margin in the open loop response, the JTF -3 dB corner frequency, with shift proportionally with the change of pattern transition density. For example, the 2.1 MHz JTF -3dB corner frequency, set with a pattern with a transition density of 0.5, will shift to 4.2 MHz when a pattern with a transition density of 1.0, such as the D10.2 pattern, is applied. A proportional decrease of the JTF -3dB corner frequency will also be observed for a decrease in pattern transition density compared to a 0.5 transition density. This is the expected JMD response to changes in pattern transition density as the reference design would exhibit. If a JMD shifts the JTF -3dB corner frequency in a manner that does not match this characteristic, or does not shift at all, measurements of jitter with patterns with transition densities significantly different than 0.5 may lead to discrepancies in reported jitter levels. In the case of reported jitter discrepancies between JMDs, the JMD with the shift of the -3dB corner frequency, closest to the proportional characteristic of the reference design, it to be considered correct. This characteristic may be measured using the conditions defined above for measuring the -3dB corner frequency, using multiple patterns with different transition densities.

Final Example Specification (3)

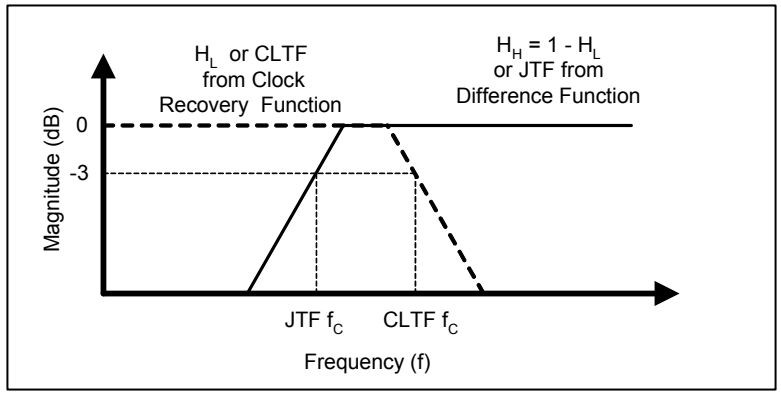
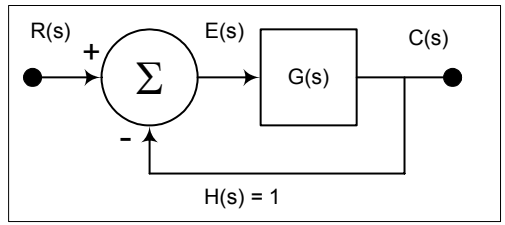


Figure 139 – Jitter at Receiver, High Pass Function
This response function JTF (HH in Figure 139) mimics the receiver's ability to track lower frequency jitter components (wander, SSC) and not include them in the jitter measurement. This measurement methodology enables any measurement instrument to accurately measure the jitter seen by a receiver and produce measurements that correlate from measurement instrument to measurement instrument.
It should be noted that the corner frequency of the JTF is not the corner frequency of the clock recovery CLTF. This may not be obvious until one considers the phase shift caused by the clock recovery circuit. In general the vector sum HL(f) + HH(f) = 1. All quantities consist of changing magnitude and phase as a function of frequency. This accounts for differences in corner frequencies and peaking in the two frequency dependant functions.

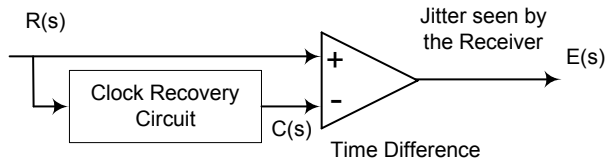
Final Example Specification (4)

Figure 140 shows more detail into how the JTF and CLTF relate to the jitter that would be applied to a receiver. The subfigure A) represents a generic control system block diagram for a feedback loop based clock recovery system. Subfigure B) translates the same complex variables to the combined system of the clock recovery circuit and the time difference function. It can be seen that E(s) is the jitter seen by the receiver, as well as being the error signal in the clock recovery circuit. Subfigure C) provides the defining equations for the clock recovery circuit CLTF and the combined system JTF function.
Both the CLTF and the JTF are uniquely defined by the open loop transfer function G(s). Defining a CLTF does not uniquely define the G(s) and subsequently the JTF due to the level of cancellation of G(s) in the numerator and denominator of the CLTF especially when G(s) is much greater than 1, which is necessary for jitter tracking by the clock recovery circuit. This is the rational for Gen2i and Gen2m directly specifying the JTF rather than the CLTF of the clock recovery circuit. When the JTF of a JMD meets the requirements specified, the JMD reported jitter levels will closer represent the jitter applied to the receiver in this reference design.

A) Generic Clock Recovery Circuit



B) Clock Recovery Circuit with Time Difference



C) Defining Equations for the JTF and the CLTF

$$JTF = \frac{E(s)}{R(s)} = \frac{1}{1 + G(s)} \qquad CLTF = \frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)}$$

Equations valid for unity gain feedback: H(s) = 1
All quantities consist of Magnitude and Phase

Future Optional JTF Enhancements

- Tighter tolerances and/or a compliance envelope or additional test frequencies could be added to the JTF Magnitude response requirements. This would add additional verification test time and possibly eliminate some classes of JMDs.
- The JTF Phase response could be defined and verified with special purpose test signals such as phase locked multi-tone PJ compositions. The JTF Phase response is not directly observable on some classes of JMDs, so directly specifying it, is not practical. Only checking the reported jitter level for a well defined and easily verifiable mixed PJ frequency test signal seems like a possible JMD verification test for JTF phase. This seems to be error prone and complex.
- Defining how the JTF BW varies with changes of Dt would provide better correlation for test patterns that have a Dt that is not close to the calibration Dt of 0.5. This may eliminate some classes of JMDs. Even with hardware clock recovery type 2 PLL based JMDs, this shift of BW with Dt varies depending on the open loop gain-phase characteristics. Tolerances must allow for differences in design strategy but must be tight enough to achieve a benefit.
- A shift to naming the jitter spectrum in terms of the JTF BW (MHz) rather than the historical CLTF BW (Fbaud/N) could be possible for future standards and JMD specifications. Informative typical CLTF BW could be included to minimize the confusion of the change of naming convention.

The present JTF requirements were chosen as a practical balance between better correlation and maintaining a wide choice of JMD classes that may be used for compliance testing. At some point, other JMD differences such as with algorithms and hardware differences, become more significant for better correlation than tightening the JTF requirements. There are diminishing returns achievable by excessive JTF definition imposed requirements.

A Quote: That's all I have to say about that. – Forrest Gump

or... The End