To: T10 Technical Committee
From: Bob Sheffield (robert.l.sheffield@intel.com)
Date: 15 March 2007
Subject: 07-148r0: SAT2 - Use something other than "comprises"

Revision history
Revision 0 (15 March 2007) First revision

Related documents
sat2-r00 - SCSI / ATA Translation-2 revision 00
07-105r2 SAM-4: Comments from Adam Richter

Overview

The CAP WG approved a proposal to fix a number of editoral errors in SAM-4, 07-105r2, in March ‘07. Among those editorial changes were changes to replace all instances of the term, “comprises” with something less ambiguous (and less mis-used). There are 4 instances of the term in SAT-2. This proposal suggests alternate text for each.

Suggested changes

3.5.2 Numeric conventions

A binary number is represented in this standard by any sequence of digits consisting ~~comprised~~ of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Underscores or spaces may be included in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b or 0_0101_1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting ~~comprised~~ of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Underscores or spaces may be included in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h or B_FD8C_FA23h).

A decimal number is represented in this standard by any sequence of digits consisting ~~comprised~~ of only the Western-Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

When the value of the bit or field is not relevant, x or xx appears in place of a specific value.

9.2.5 DCRT bit

If the DCRT bit is set to zero and media certification is supported by the SATL, then the SATL shall issue ATA verify commands (see 3.1.23) to access all the logical sectors on the medium of the ATA device that ~~comprise every logical block emulated by the SATL~~ the SATL uses to emulate logical blocks accessible by the application client. For every unrecoverable read error that is encountered, the SATL shall issue an ATA write command (see 3.1.25) to the defective logical sector to attempt to cause logical sector reallocation. The data written shall be the data pattern specified by the initialization pattern descriptor, if any, or vendor-specific. After writing the affected logical sector, the SATL shall again issue an ATA verify command to the same logical sector to verify the alternate logical sector is not defective. The process (e.g., verify, write, verify, write, etc.) shall repeat until the logical sector is verified successfully or the disk returns a fatal error other than an unrecoverable read error (e.g., device fault). See 5.3 for a description of error handling for multiple ATA command sequences.